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APPLICATION NOTE 202

NV SRAM Frequently Asked Questions

May 14, 2002

Abstract: This application note discusses theory of operation and application of NV SRAMs such as the DS1220, DS1225, and DS1230. First it discusses NV SRAM module construction, with an overview of the battery, controller, and SRAM that is used in a typical device. Application information regarding interconnects to popular 8-bit Motorola® and Intel® bus structures is shown in block diagram form. Answers to common questions regarding issues found during the design, test, manufacture, and use of NV SRAMs in electronic systems is explained in detail. Information on some older and obsolete parts is discussed with recommendations on pin-for-pin replacements with more contemporary devices.

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What Is an NV SRAM?

A nonvolatile static random access memory (NV SRAM) is a type of computer memory that maintains its data when power is shut off. NV SRAMs store digital information like system configuration or temporarily store transient digital data, such as what passes through a telecom router, so that it can be recovered in case of a power failure.

An NV SRAM is a nonvolatile memory module built using a standard SRAM, an integrated circuit (IC) controller with a battery switchover circuit, and a lithium battery. All of these components are mounted on a circuit board and encapsulated in a plastic tub. The example below (**Figure 1**) is pinned out to match the footprint and pinout of a JEDEC-standard SRAM so that the two can be used interchangeably.
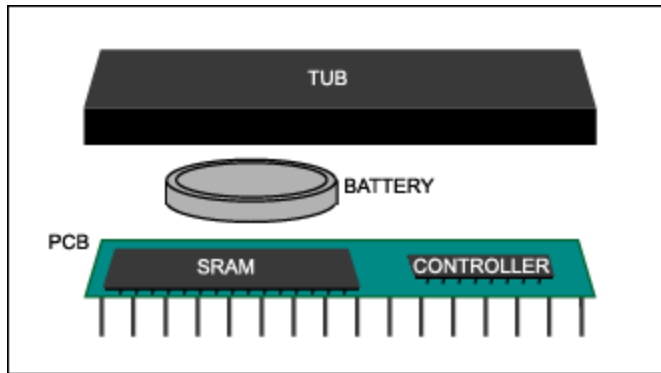
Figure 1. JEDEC-standard SRAM.

A typical NV SRAM consists of a DS1210 (or similar) nonvolatile controller chip, a lithium coin-cell battery, and a screened, low-standby current SRAM. The DS1210 used in this example is identical to the MXD1210. The controller, in conjunction with the battery, converts the CMOS SRAM into nonvolatile memory.

The DS1210 controller performs two functions. First, it switches between V_{CC} and the lithium battery, depending on the power situation. It also gates the chip-enable signal used to enable the SRAM, allowing access to the SRAM during conditions of good power and inhibiting access to the SRAM during conditions of power-up or power-down.

The DS1210 monitors power for an out-of-tolerance condition. When such a condition is detected, active-low CE is inhibited to the SRAM, which write-protects the device as the circuit powers down. At the point when V_{CC} is at the same level as the internal battery voltage, the controller switches SRAM over to one of the two batteries that has the highest voltage and fullest charge. This maintains the memory contents in the SRAM until the next power-up. During power-up, active-low CE is maintained high (SRAM inactive) until power is stable for 125ms (max). After that, the NV SRAM can be accessed as if it were a normal SRAM part.
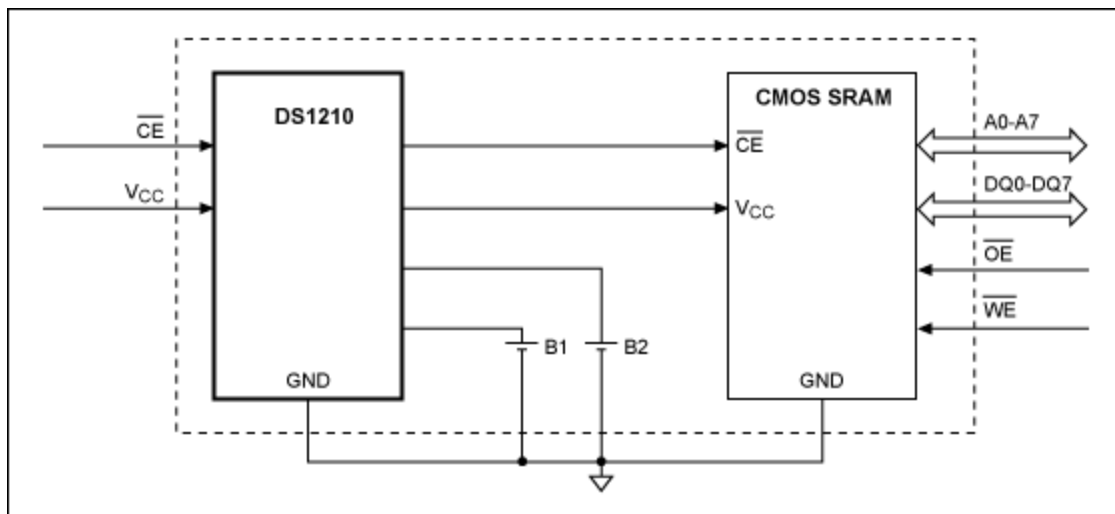

Figure 2. NV SRAM block diagram.

How Do I Interface to an NV SRAM?

The two most common types of NV SRAMs application interfaces are shown below with the DS80C320 and HC68000 examples. The 8051 has a multiplexed address/data bus that must be demultiplexed before applied to the NV SRAM. The HC68000 uses a demultiplexed bus, but has different control pins and bus timing for performing memory accesses. The NV SRAMs are designed to be compatible with both types of bus architecture, but need to be configured correctly.
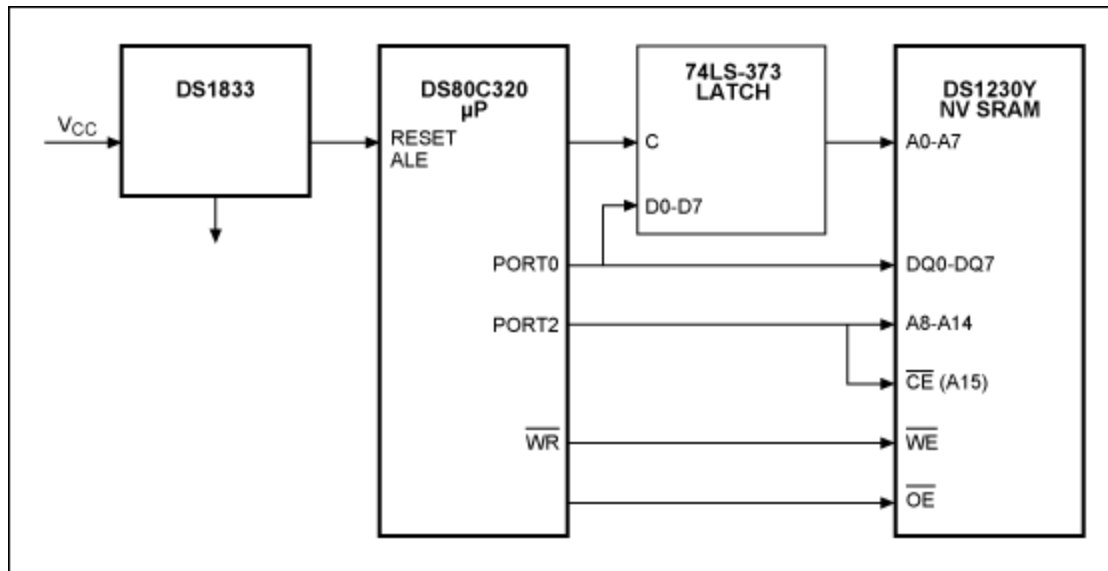

Figure 3. NV SRAM interfaced to the DS80C320.

In a typical DS80C320 to SRAM application, the designer often uses a configuration very similar to that in **Figure 3**, with the exception that active-low CE is permanently tied low. This works quite well with an SRAM, but active-low CE should not be tied low when using an NV SRAM.

A mechanism in the DS1210 controller ensures that the last active-low CE is gated through to the SRAM and returns high before actively forcing it high. This prevents partial writes and potential data corruption during the power-down cycle. If active-low CE is tied low, however, the controller waits until the battery switch-over time to disable the SRAM. This happens at a much lower voltage than normal.

During power-down, decaying power on the address, data, and control lines can be interpreted as random bits. With active-low CE tied low, the conditions can be met so that this random data is interpreted as a write cycle, corrupting the memory.

In Figure 3, a CPU supervisor resets the microcontroller at a 5% level, forcing active-low CE high and ensuring that active-low CE remains high for the reset of the power-down cycle.

Note: Application note 57, "DS80C320 Memory Interface Timing," contains information on latch selection as well as memory access requirements for the DS80C320 operating at various speeds.

The interconnect for the Motorola MC68000 family of microprocessors is shown in **Figure 4**. In eneral, this interconnect scheme works for other Motorola microprocessors.
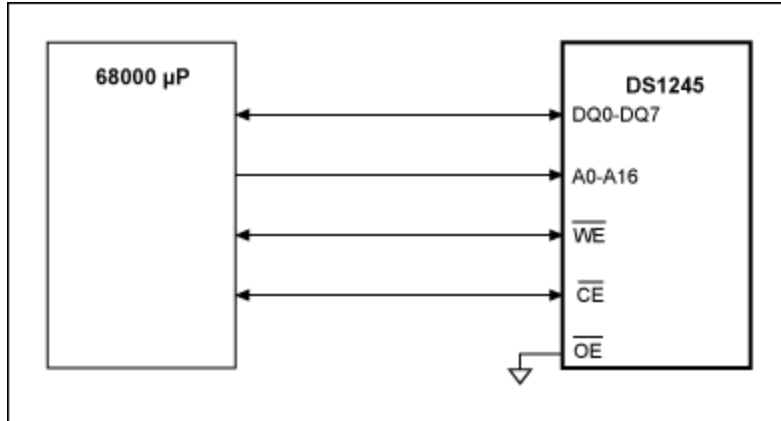
Figure 4. NV SRAM Interfaced to 68000.

Can You Turn the Freshness Seal Back On Once Power Has Been Applied?

(Most NV SRAMS have a freshness seal that isolates the battery from the NV SRAM until it first powers up. This extends the NV SRAM battery's shelf life by removing the SRAM load from the battery until it is installed in the customer's equipment and power cycled.)

No. Controlling the freshness seal requires specialized test equipment that the end user does not have.

The only exception to the rule is the PowerCap. Resetting the freshness seal is accomplished by removing the DS9034 cap, waiting sufficient time for the controller to bleed down internally (approximately 30 seconds), and then installing a new cap (reusing an old cap is not recommended).

Can you Measure the Battery Voltage of an NV SRAM?

With the exception of PowerCaps with exposed battery contacts, it is not possible to directly measure the voltage of the NV SRAM battery.

Since Flash Memory Is a Lot Cheaper, Why Not Use It Instead of NV SRAM?

When high-speed, read/write capability is needed (as in digital communication equipment), NV SRAM is the only choice. Flash can be read quickly, but generally takes a long time to write. Also, NV SRAM is the only solution if unlimited write cycles are needed. Flash, as well as other memory types, have wear-out mechanisms that limit the number of write cycles. Flash also is limited to block writes, while NV SRAM allows reading and writing to individual bytes of memory.

Are 3.3V Parts Available?

Yes. We have devices ranging from 256kb to 16Mb. Through-hole and surface-mount parts are available. The 3.3V devices are indicated by a "W" in the postfix. For a selection guide for these and other NV SRAMs visit the link below: http://para.maximintegrated.com/compare.asp?Fam=Memory&Tree=Memory&HP=Memory.cfm

Are Maxim NV SRAMs UL Recognized?

Yes. Conditions of acceptability for all modules can be found at the link below:
http://www.maximintegrated.com/TechSupport/QA/module.htm

What Other Functions Are Available on NV SRAMs?

The DS13xx series of NV SRAMs (DS1330, DS1345, DS1350) have a power-on reset output that can be used to sequence the control of the NV SRAM and the processor during power-up and power-down cycles.

Additionally, the DS13xx series performs periodic monitoring of the battery voltage and provides a discrete warning output to alert the system of impending battery failure. For a detailed description of the battery monitoring, see application note 3254, "Battery Monitoring in NV SRAM Modules."

What Replacement Parts Should I Use for the DS16xx Series of NV SRAMs?

The DS1xx* series of NV SRAMs was identical in function, package, and pinout to the DS12xx series of NV SRAMs, with the exception that it had the addition capability to write-protect individual blocks of memory. An equivalent-density DS12** series NV SRAM will work in the socket, but the block write-protect function is not available. Hardware and firmware modifications may be required.

Why Is the Battery in My DS1213 SmartSocket Dead?

(The SmartSocket was a socket for standard SRAMs that contained the controller and battery found in NV SRAM. When used with an SRAM, it is functionally identical to a NV SRAM.)

There are two common causes of this problem. First, most water-based circuit board washes, even those using de-ionized water, can leave conductive metal traces plated on the internal circuit board between the terminals of the battery. This puts an excessive load on the battery draining it. The most effective solution is to replace the socket and SRAM with a comparable NV SRAM.

Second, when using a SmartSocket, it is the customer's responsibility to procure SRAM that has a maximum (not typical) standby current of less than 1µA. This will give the SmartSocket an estimated lifetime of 10 years, given the capacity of the batteries we use internally in the SmartSocket assembly. The customer can eliminate the problem of procuring low-current dual-in-line SRAMs by using a comparable NV SRAM.

A conversion procedure for replacing SmartSockets is detailed in application note 4392, "How to Replace a DS1213 SmartSocket with an Equivalent-Density NV SRAM Module."

I Replaced My Standard SRAM with an NV SRAM and Now My System Doesn't Work at All. What Caused This?

In general, this is caused by one of two things:

First, the designer may not have considered the recovery time, or t_{REC}, of the particular NV SRAM selected. On power-up, an internal power monitor disables the NV SRAM until a power-good situation and then holds it disabled for an additional 2ms (max) or 125ms (max), depending on the NV SRAM

after power-good. If the microcontroller attempts to access the memory before t_{REC} times out, it will not be able to access the device's memory to read or write, so the system fails. Either a software loop on power-up to extend the access time past t_{REC}, or moving the NV SRAM access somewhere later in the power-on initialization sequence in the microcontroller's firmware will resolve the problem. This problem often can be corrected by selecting a CPU supervisor that has a reset time longer than the recovery time of the NV SRAM.

Second, selecting the voltage levels at which the NV SRAM and the microcontroller become active is critical. If the microcontroller becomes active below 4.5V, and the NV SRAM becomes active above 4.75V, the same problem of the microcontroller trying to access a disabled NV SRAM occurs. The power-good threshold for the two devices should force the system to enable the NV SRAM first and then the processor. This involves selecting the NV SRAM with the appropriate power-good level and pairing that with a CPU supervisor that enables the processor at a higher voltage.

Some NV SRAMs have an active-low RESET output that is synchronous with its own internal reset. If this is used to reset the microcontroller, the possibility of trying to access a disabled NV SRAM is removed.

Why Am I Getting Data Corruption in My NV SRAM?

The most common cause of corruption is electrical. Negative voltage spikes on any pin, especially when powered down, can cause data corruption. ESD protection diodes on the I/O cause the internal V_{CC} to drop lower than the data-retention level, thus causing data loss. The only way to prevent this from happening is to determine and eliminate the cause of the negative voltage spikes. The same is true for the power input. Some older linear regulators, when configured with a large output decoupling cap, have outputs that go negative when going through power cycles.

Voltages applied to the I/O of the NV SRAM when powered down can cause the NV SRAM to remain inactive when powered up. These voltages on the unpowered part turn on the ESD protection diodes as well, which puts a charge on the internal V_{CC} substrate that is greater than the battery voltage. The switchover from battery to external V_{CC} occurs when the external V_{CC} is greater. If they are the same level, the switchover never occurs and the NV SRAM remains in the shutdown mode. The only way to resolve this is to correct the design so that no I/O pins are active when the device is powered down.

What's a DS1235?

A number of years ago, Dallas Semiconductor® had a 256kb NV SRAM product called the DS1235. It was functionally and physically identical to the DS1230, with the exception that the DS1235 had a five-year data-retention expectation instead of 10 years. An alternative is the DS1230 with the same power-supply tolerance, and with a performance rating *equal to or faster than* the original DS1235 product (for example, the DS1235Y-150 should be replaced by a DS1230Y-70+).

What Does the "-200" Mean, and Why Are Those Products Unavailable?

The performance, or speed grade, of an NV SRAM indicates the maximum time required for the NV SRAM to present data upon a read request. A "-200" represents a 200ns access, which was the typical performance at the time of product introduction. With design and process improvements over time, memory-component performance has been significantly improved, to the point where 200ns component are no longer readily available.

When replacing an older NV SRAM product, it may be necessary to substitute a higher-performance component in place of the older 200ns (or 150ns or 120ns) version. A memory product that is rated to present data in no more than 70ns ("-70") can easily exceed the system requirements of the old -200. For more information on performance-based substitutions, refer to applications note 4893, "Substitution Rules for Nonvolatile Memory Components."

What's an LPM?

Many years ago, Dallas Semiconductor had offered a "low-profile module," which was a single-piece 34-pin module package that *required a custom socket* for board mounting. The sockets subsequently became unavailable, which led to discontinuation of this package type.

Replace a low-profile module and its custom socket with an SMT-compatible PowerCap product of equivalent function (for example, the DS1230YL-100 should be replaced by a DS1230YP-70+ and a DS9034PC+ battery cap).

Are Any NV SRAMs Not Recommended for Future Designs?

Yes. The DS1220Y and DS1225Y are not recommended for new designs. These older devices used a battery reference to determine the power-valid trip-point during power cycles. Newer designs use a band gap reference. The battery-referenced devices had a trip point that decreased during the life of the device. Devices using the band gap have a trip point that is stable for the life of the product.

The DS1220AD and DS1225AD are recommended for new designs needing the functionality of a 16kb or 64kb NV SRAM. For existing designs, the DS1220AD or DS1225AD may be considered as replacements; however, the "Y" parts had a reset timeout on the order of milliseconds while the "AD" parts have a timeout of 125ms. When replacing the Y part with the AD part, it must be determined that the controlling processor does not become active during a power-up cycle for at least 125ms to ensure that the NV SRAM is available before the processor attempts a memory access.

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Related Parts		
DS1210	Nonvolatile Controller Chip	Free Samples
DS1218	Nonvolatile Controller	
DS1220AB	16k Nonvolatile SRAM	Free Samples
DS1220AD	16k Nonvolatile SRAM	Free Samples
DS1225AB	64k Nonvolatile SRAM	Free Samples
DS1225AD	64k Nonvolatile SRAM	Free Samples
DS1230AB	256k Nonvolatile SRAM	Free Samples
DS1230W	3.3V 256k Nonvolatile SRAM	Free Samples
DS1230Y	256k Nonvolatile SRAM	Free Samples

DS1245AB	1024k Nonvolatile SRAM	Free Samples
DS1245W	3.3V 1024k Nonvolatile SRAM	Free Samples
DS1245Y	1024k Nonvolatile SRAM	Free Samples
DS1249AB	2048k Nonvolatile SRAM	Free Samples
DS1249W	3.3V 2048kb Nonvolatile SRAM	Free Samples
DS1249Y	2048k Nonvolatile SRAM	Free Samples
DS1250AB	4096k Nonvolatile SRAM	Free Samples
DS1250W	3.3V 4096k Nonvolatile SRAM	Free Samples
DS1250Y	4096k Nonvolatile SRAM	Free Samples
DS1265AB	8M Nonvolatile SRAM	Free Samples
DS1265W	3.3V 8Mb Nonvolatile SRAM	Free Samples
DS1265Y	8M Nonvolatile SRAM	Free Samples
DS1270AB	16M Nonvolatile SRAM	Free Samples
DS1270W	3.3V 16Mb Nonvolatile SRAM	Free Samples
DS1270Y	16M Nonvolatile SRAM	Free Samples
DS1312	Nonvolatile Controller with Lithium Battery Monitor	Free Samples
DS1314	3V Nonvolatile Controller with Lithium Battery Monitor	Free Samples
DS1321	Flexible Nonvolatile Controller with Lithium Battery	Free Samples
DS1323	3.3V Flexible Nonvolatile Controller with Lithium Battery Monitor	
DS1330AB	256k Nonvolatile SRAM with Battery Monitor	Free Samples
DS1330W	3.3V 256k Nonvolatile SRAM with Battery Monitor	Free Samples
DS1330Y	256k Nonvolatile SRAM with Battery Monitor	Free Samples
DS1345AB	1024k Nonvolatile SRAM with Battery Monitor	Free Samples
DS1345W	3.3V 1024k Nonvolatile SRAM with Battery Monitor	Free Samples
DS1345Y	1024k Nonvolatile SRAM with Battery Monitor	Free Samples
DS1350AB	4096k Nonvolatile SRAM with Battery Monitor	Free Samples
DS1350W	3.3V 4096K Nonvolatile SRAM with Battery Monitor	Free Samples
DS1350Y	4096k Nonvolatile SRAM with Battery Monitor	Free Samples

More Information