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APPLICATION NOTE 3121

Selecting a T1/E1/J1 Single-Chip Transceiver

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Abstract: This article, originally published in the October 2003 issue of Electronic Products magazine, discusses how to select a T1/E1/J1 single-chip transceiver (SCT).

Introduction

T and E Carrier networks have come a long way since the T Carrier's introduction in the 1960s. Today, the designer will find many features that have been integrated into the T1/E1/J1 single-chip transceiver (SCT).

Due to the numerous functions a transceiver can incorporate, this article will highlight some of the important features that designs require.

T, E, and J Carrier Networks

T1 at 1.544Mbps is the lowest rate of the T Carrier hierarchy for digital multiplexed transmission across the North American Public Switched Telephone Network (PSTN). It was originally designed to transport digitized voice. T1 uses pulse code modulation and time-division multiplexing to transport up to 24 channels of carrier grade voice, called DS0s. Each DS0 or timeslot carries up to 64kbps of information.

E1 is a European digital transmission format that carries up to 32 channels of voice whose multiplexed clock rate is 2.048Mbps.

Today, not only voice can be transported over a T1 or E1 line, but data as well, or a combination of both. T1 and E1 lines are used extensively in applications such as cellular base stations, business access routers, and private branch exchanges. **Figure 1** shows a functional block diagram of a typical T1/E1/J1 SCT. Note: J1 is a variant of T1 that is used exclusively in Japan.

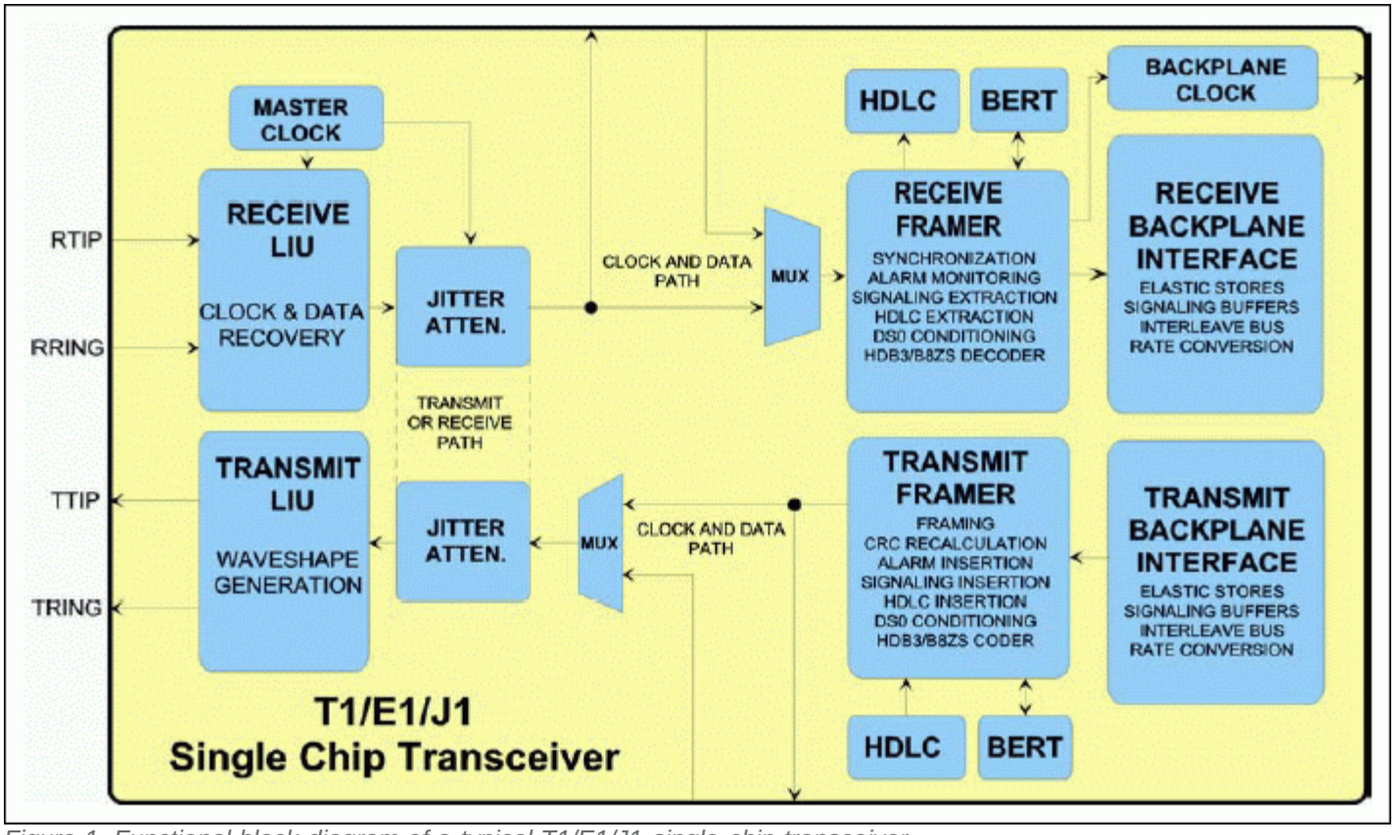

Figure 1. Functional block diagram of a typical T1/E1/J1 single-chip transceiver.

Line Interface Unit and Framer

The line interface unit (LIU) of the SCT is the physical interface to the copper loop. The framer synchronizes to the data that is received from the LIU, as well as formats the data for the LIU to transmit. An advantage in some SCTs is the LIU can offer operation for both short haul and long haul. This allows the SCT to be used in applications for digital signal cross-connect Level 1 (DSX-1) filtering for CSU (channel service unit)/DSU (data service unit).

In a traditional T1/E1/J1 design, the LIU and framer would be separate ICs. However, very large-scale integration technology has allowed both parts to be combined onto a single silicon substrate. One feature to look for in a SCT is direct access to signals between the LIU and framer. This allows for functions, such as modifying the data stream or inserting code from an external source. Another benefit is the ability to tap bipolar streams for monitoring purposes.

Software Programmable Line Termination

Given the international nature of T1/E1/J1 equipment use, programmable software termination of the copper loop is a useful feature that Dallas Semiconductor started with the DS2155 SCT. The engineer can design a complete T1/E1/J1 board and change the line termination required on the copper loop, via software, without changing any external components. Today, this feature has become a standard requirement, since most new T1/E1/J1 designs are cost sensitive.

Jitter Attenuator

T/E Carrier loops can exhibit moments of desynchronization from time to time. This phenomenon is often a consequence of jitter. Jitter is defined as the magnitude of phase variation, with respect to an ideal reference clock whose frequency

of variation is greater than 10Hz.

To maximize robustness and clock reusability, choose a SCT that offers jitter attenuation that can be applied to the transmit or receive path. Some products also offer two jitter attenuation buffer depths for applications that require robust operation with large jitter present or that require lower latency.

High-Level Data Link Control

High-Level Data Link Control (HDLC) is a type of layer 2 processing in the ISO 7-layer model. Physical link maintenance and quality monitoring are typical applications of HDLC controllers. For more flexibility, choose HDLC controllers that can be assigned to single or multiple DSOs, or facility data link (FDL) bits.

Bit Error-Rate Tester (BERT)

Communication channels need diagnostic tools for testing the link quality. It is common for SCTs to include a transmit and receive BERT, which can inject a pseudo-random data pattern from the transmit side into the copper loop. The receiver BERT can then synchronize to this signal. The signal can be attenuated and/or noise can be injected into the loop while the BERTs are running. This can help characterize the network consisting of the SCT, copper loop, and higher layers of software. If errors are detected at the BERT level, then the communication channel may need further investigation.

Protection Switching

With T/E lines delivering vital data, many designs require a backup solution if the copper loop becomes compromised or if the line card ceases to work properly. Protection switching allows a backup SCT to come online in place of the failing SCT, without losing frame synchronization. Many solutions that offer this feature do not require external relays or switches. LIUs with high-impedance receiver inputs and transmitter outputs that can be tri-stated are ideal for use in protection switching.

Multiport Densities

Most T/E Carrier line cards today are multiport. One reason for multiport designs is that the need for bandwidth is larger than 1.544Mbps or 2.048Mbps. In this case, the T1s or E1s are bonded together or logically combined as a single unit, such as in Multilink Frame Relay. Another application that commonly uses multiport line cards is Inverse Multiplexing ATM (IMA). With this type of demand from the end customer, SCTs are now available in multiport densities in a single package.

Low-Voltage Supplies

Framers and LIU products have traditionally required +5V supplies. Today, most offerings emphasize low power and require a single supply of 3.3V and are 5V IO tolerant.

Related Parts		
DS21352	3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers	
DS21354	3.3V/5V E1 Single Chip Transceivers (SCT)	
DS2155	T1/E1/J1 Single-Chip Transceiver	Free Samples
DS21552	3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers	

DS21554	3.3V/5V E1 Single Chip Transceivers (SCT)	Free Samples
DS2156	T1/E1/J1 Single-Chip Transceiver TDM/UTOPIA II Interface	Free Samples
DS2196	T1 Dual Framer LIU	
DS21Q352	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q354	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q50	Quad E1 Transceiver	
DS21Q55	Quad T1/E1/J1 Transceiver	
DS21Q552	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q554	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q58	E1 Quad Transceiver	
DS21Q59	E1 Quad Transceiver	

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