

C3M0015065K

Silicon Carbide Power MOSFET

C3M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- C3M™ SiC MOSFET technology
- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

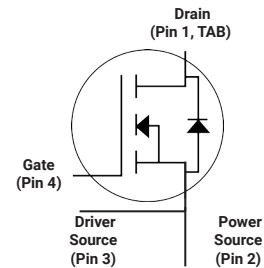
Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- EV chargers
- Solar inverters
- UPS
- SMPS
- DC/DC converters

Package



| Part Number | Package | Marking |
|-------------|----------|-------------|
| C3M0015065K | TO 247-4 | C3M0015065K |

Maximum Ratings ($T_c=25^\circ\text{C}$, unless otherwise specified)

| Symbol | Parameter | Value | Unit | Note |
|----------------|--|-------------|------------------|-------------------|
| V_{DSmax} | Drain - Source Voltage | 650 | V | |
| V_{GSmax} | Gate - Source voltage | -8/+19 | V | Note 1 |
| I_D | Continuous Drain Current, $V_{GS} = 15\text{ V}$, $T_c = 25^\circ\text{C}$ | 120 | A | Fig. 19 Note 2 |
| | Continuous Drain Current, $V_{GS} = 15\text{ V}$, $T_c = 100^\circ\text{C}$ | 96 | | |
| $I_{D(pulse)}$ | Pulsed Drain Current, Pulse width t_p limited by T_{jmax} | 418 | A | |
| P_D | Power Dissipation, $T_c=25^\circ\text{C}$, $T_j = 175^\circ\text{C}$ | 416 | W | Fig. 20 |
| T_J, T_{stg} | Operating Junction and Storage Temperature | -40 to +175 | $^\circ\text{C}$ | |
| T_L | Solder Temperature, 1.6mm (0.063") from case for 10s | 260 | $^\circ\text{C}$ | |
| M_d | Mounting Torque, (M3 or 6-32 screw) | 1 | Nm lbf-in | |
| | | 8.8 | | |

Note (1): Recommended turn off / turn on gate voltage $V_{GS} = -4V...0V / +15V$

Note (2): Package limited to 120 A

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|---------------|---|------|------|------|---------------|--|---------------|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | 650 | | | V | $V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$ | |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.8 | 2.3 | 3.6 | V | $V_{DS} = V_{GS}, I_D = 15.5\ \text{mA}$ | Fig. 11 |
| | | | 1.9 | | V | $V_{DS} = V_{GS}, I_D = 15.5\ \text{mA}, T_J = 175^\circ\text{C}$ | |
| I_{DSS} | Zero Gate Voltage Drain Current | | 1 | 50 | μA | $V_{DS} = 650\ \text{V}, V_{GS} = 0\ \text{V}$ | |
| I_{GSS} | Gate-Source Leakage Current | | 10 | 250 | nA | $V_{GS} = 15\ \text{V}, V_{DS} = 0\ \text{V}$ | |
| $R_{DS(on)}$ | Drain-Source On-State Resistance | 10.5 | 15 | 21 | m Ω | $V_{GS} = 15\ \text{V}, I_D = 55.8\ \text{A}$ | Fig. 4, 5, 6 |
| | | | 20 | | | $V_{GS} = 15\ \text{V}, I_D = 55.8\ \text{A}, T_J = 175^\circ\text{C}$ | |
| g_{fs} | Transconductance | | 42 | | S | $V_{DS} = 20\ \text{V}, I_{DS} = 55.8\ \text{A}$ | Fig. 7 |
| | | | 40 | | | $V_{DS} = 20\ \text{V}, I_{DS} = 55.8\ \text{A}, T_J = 175^\circ\text{C}$ | |
| C_{iss} | Input Capacitance | | 5011 | | pF | $V_{GS} = 0\ \text{V}, V_{DS} = 400\ \text{V}$ $f = 100\ \text{KHz}$ $V_{AC} = 25\ \text{mV}$ | Fig. 17, 18 |
| C_{oss} | Output Capacitance | | 289 | | | | |
| C_{rss} | Reverse Transfer Capacitance | | 31 | | | | |
| $C_{o(er)}$ | Effective Output Capacitance (Energy Related) | | 357 | | | | Note: 3 |
| $C_{o(tr)}$ | Effective Output Capacitance (Time Related) | | 516 | | | | Note: 3 |
| E_{oss} | C_{oss} Stored Energy | | 29 | | | | μJ |
| E_{ON} | Turn-On Switching Energy (Body Diode) | | 401 | | μJ | $V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 55.8\ \text{A},$ $R_{G(ext)} = 5\ \Omega, L = 57.6\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode of MOSFET | Fig. 25 |
| E_{OFF} | Turn Off Switching Energy (Body Diode) | | 254 | | | | |
| E_{ON} | Turn-On Switching Energy (External Diode) | | 234 | | μJ | $V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 55.8\ \text{A},$ $R_{G(ext)} = 5\ \Omega, L = 57.6\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = External SiC DIODE | Fig. 25 |
| E_{OFF} | Turn Off Switching Energy (External Diode) | | 303 | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | | 23 | | ns | $V_{DD} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 55.8\ \text{A}, R_{G(ext)} = 5\ \Omega, L = 57.6\ \mu\text{H}$ Timing relative to V_{DS} Inductive load | Fig. 26 |
| t_r | Rise Time | | 32 | | | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | 57 | | | | |
| t_f | Fall Time | | 15 | | | | |
| $R_{G(int)}$ | Internal Gate Resistance | | 1.5 | | Ω | $f = 1\ \text{MHz}, V_{AC} = 25\ \text{mV}$ | |
| Q_{gs} | Gate to Source Charge | | 53 | | nC | $V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 55.8\ \text{A}$ Per IEC60747-8-4 pg 21 | Fig. 12 |
| Q_{gd} | Gate to Drain Charge | | 58 | | | | |
| Q_g | Total Gate Charge | | 188 | | | | |

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{ds} is rising from 0 to 400V
 $C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{ds} is rising from 0 to 400V

Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Typ. | Max. | Unit | Test Conditions | Note |
|----------------|----------------------------------|------|------|------|---|---------------|
| V_{SD} | Diode Forward Voltage | 4.7 | | V | $V_{GS} = -4\text{ V}, I_{SD} = 27.9\text{ A}, T_J = 25^\circ\text{C}$ | Fig. 8, 9, 10 |
| | | 4.2 | | V | $V_{GS} = -4\text{ V}, I_{SD} = 27.9\text{ A}, T_J = 175^\circ\text{C}$ | |
| I_S | Continuous Diode Forward Current | | 79 | A | $V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$ | |
| $I_{S, pulse}$ | Diode pulse Current | | 223 | A | $V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{jmax} | |
| t_{rr} | Reverse Recover time | 22 | | ns | $V_{GS} = -4\text{ V}, I_{SD} = 55.8\text{ A}, V_R = 400\text{ V}$ $dif/dt = 4000\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$ | |
| Q_{rr} | Reverse Recovery Charge | 510 | | nC | | |
| I_{rrm} | Peak Reverse Recovery Current | 39 | | A | | |
| t_{rr} | Reverse Recover time | 26 | | ns | $V_{GS} = -4\text{ V}, I_{SD} = 55.8\text{ A}, V_R = 400\text{ V}$ $dif/dt = 2500\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$ | |
| Q_{rr} | Reverse Recovery Charge | 432 | | nC | | |
| I_{rrm} | Peak Reverse Recovery Current | 28 | | A | | |

Thermal Characteristics

| Symbol | Parameter | Typ. | Unit | Test Conditions | Note |
|-----------------|---|------|---------------------------|-----------------|---------|
| $R_{\theta JC}$ | Thermal Resistance from Junction to Case | 0.35 | $^\circ\text{C}/\text{W}$ | | Fig. 21 |
| $R_{\theta JA}$ | Thermal Resistance From Junction to Ambient | 40 | | | |



Typical Performance

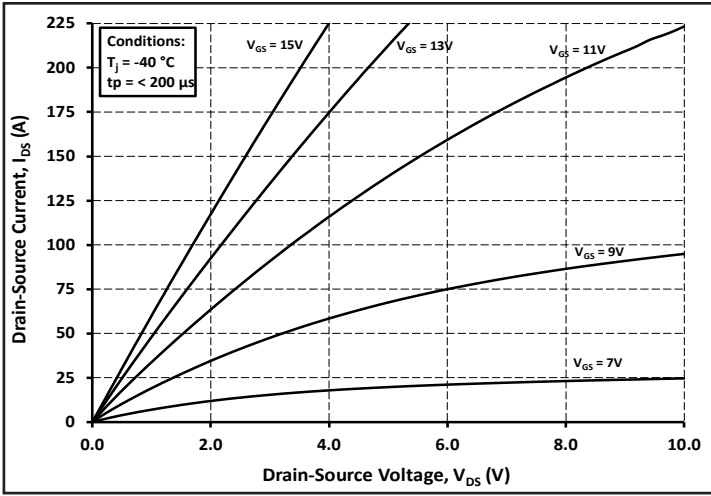


Figure 1. Output Characteristics $T_j = -40\text{ }^\circ\text{C}$

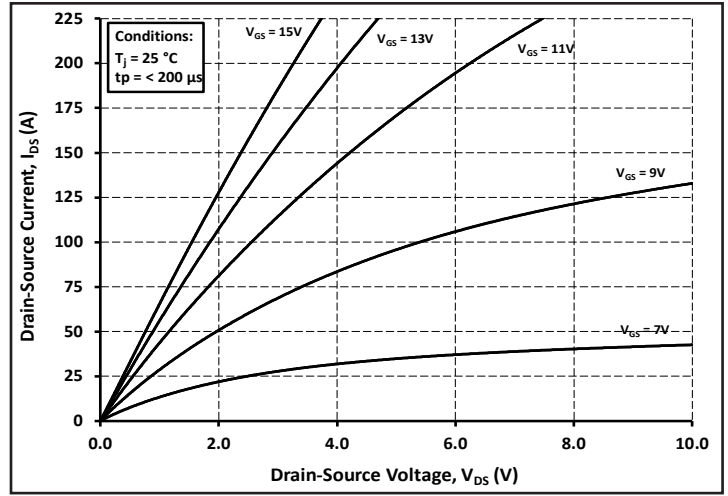


Figure 2. Output Characteristics $T_j = 25\text{ }^\circ\text{C}$

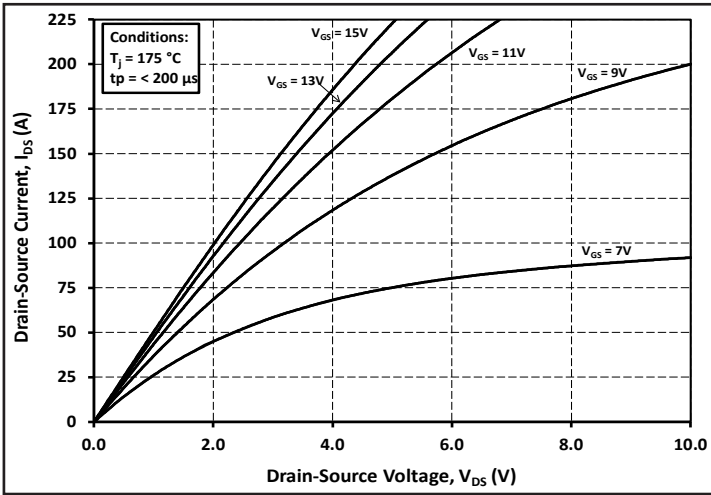


Figure 3. Output Characteristics $T_j = 175\text{ }^\circ\text{C}$

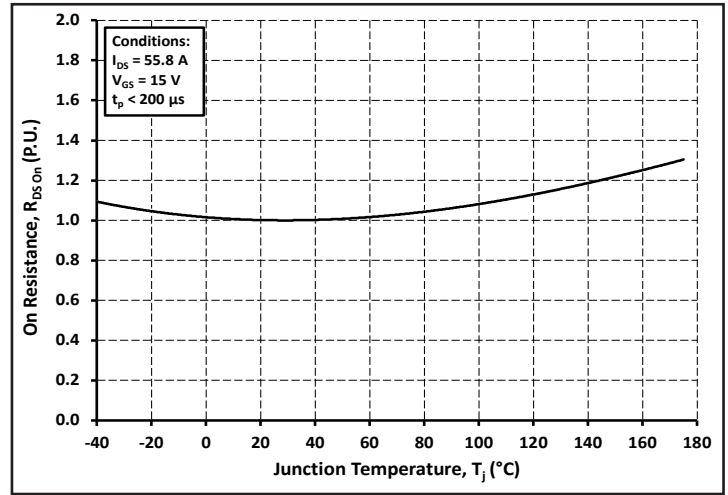


Figure 4. Normalized On-Resistance vs. Temperature

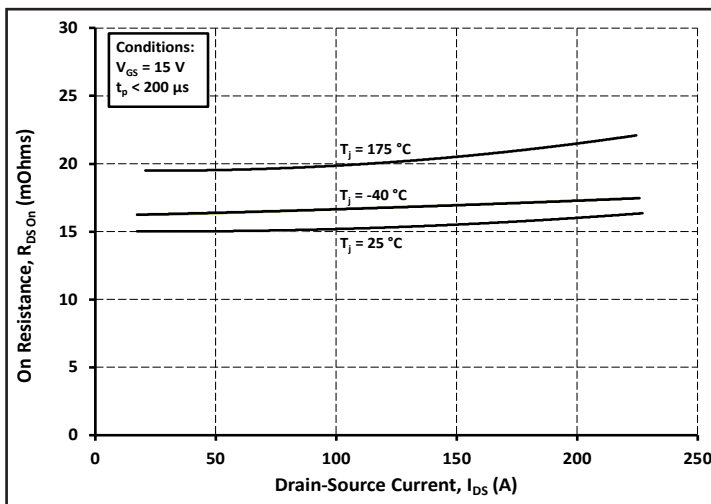


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

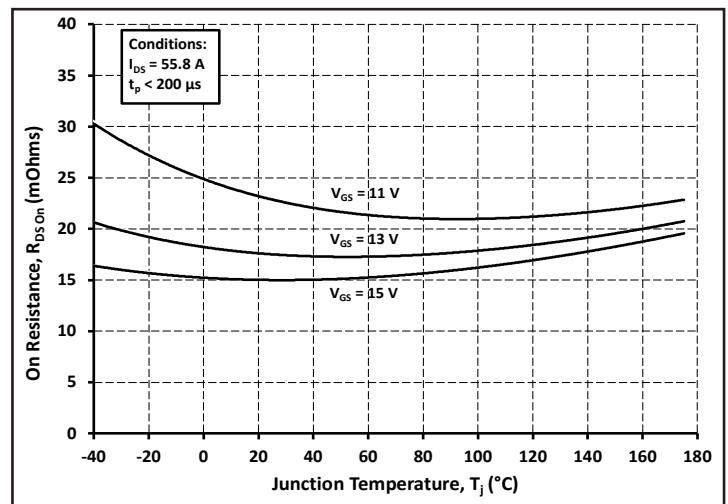


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

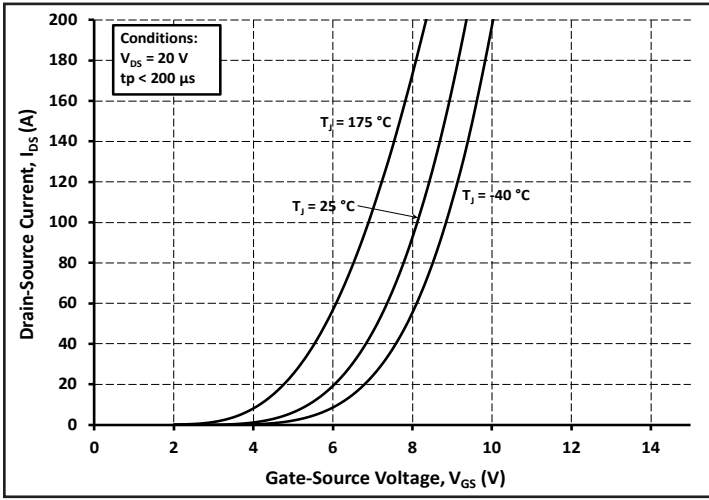


Figure 7. Transfer Characteristic for Various Junction Temperatures

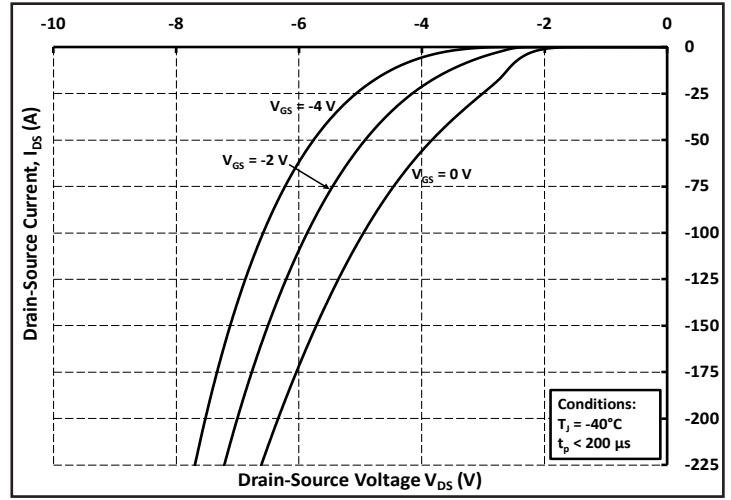


Figure 8. Body Diode Characteristic at -40 °C

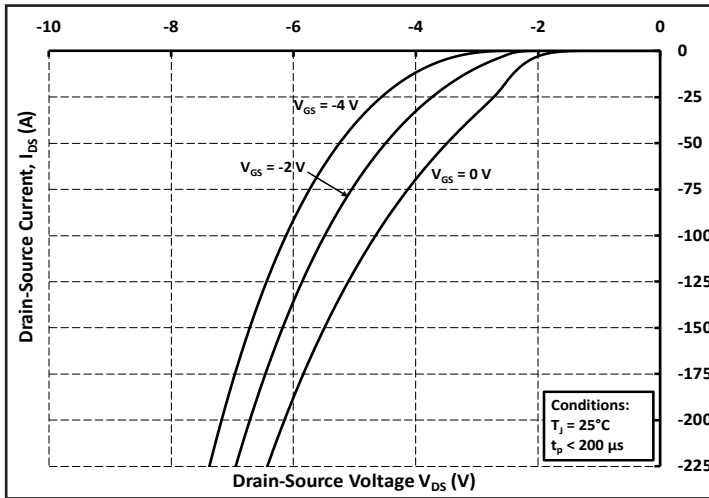


Figure 9. Body Diode Characteristic at 25 °C

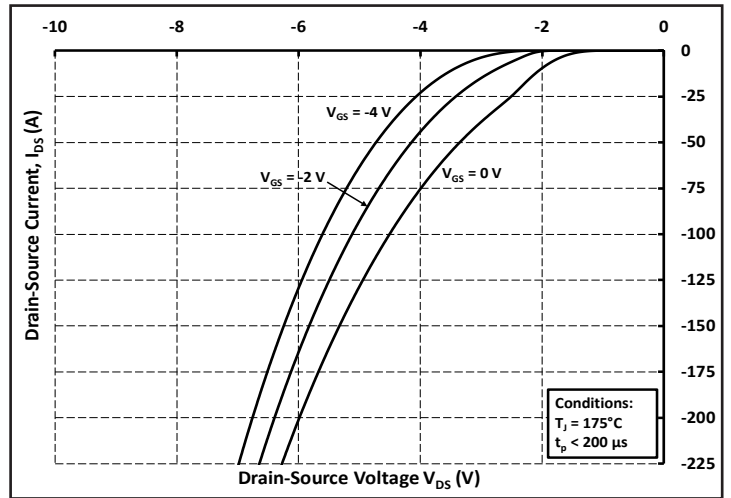


Figure 10. Body Diode Characteristic at 175 °C

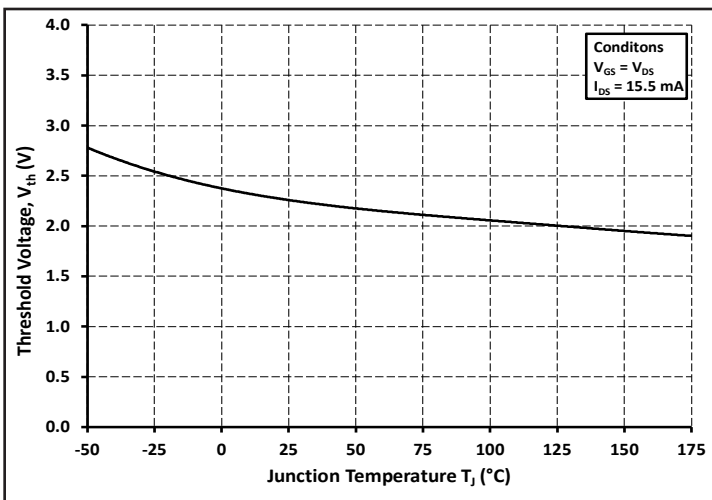


Figure 11. Threshold Voltage vs. Temperature

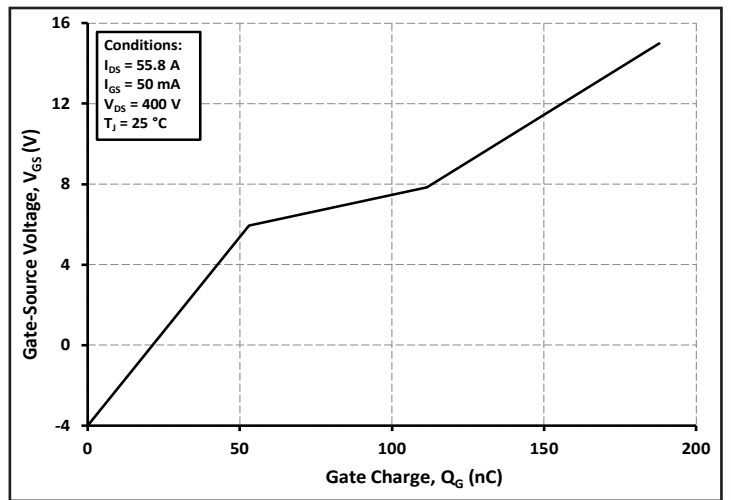


Figure 12. Gate Charge Characteristics



Typical Performance

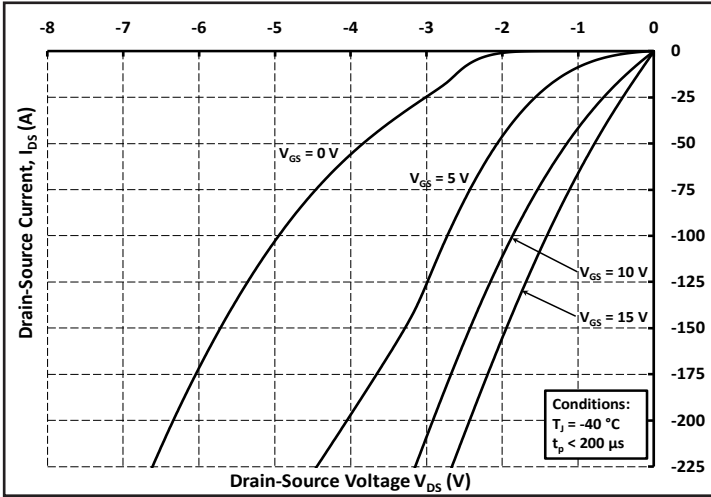


Figure 13. 3rd Quadrant Characteristic at -40 °C

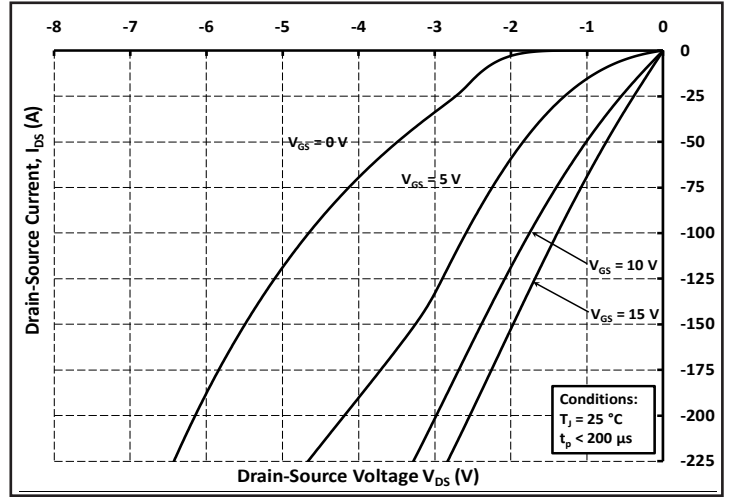


Figure 14. 3rd Quadrant Characteristic at 25 °C

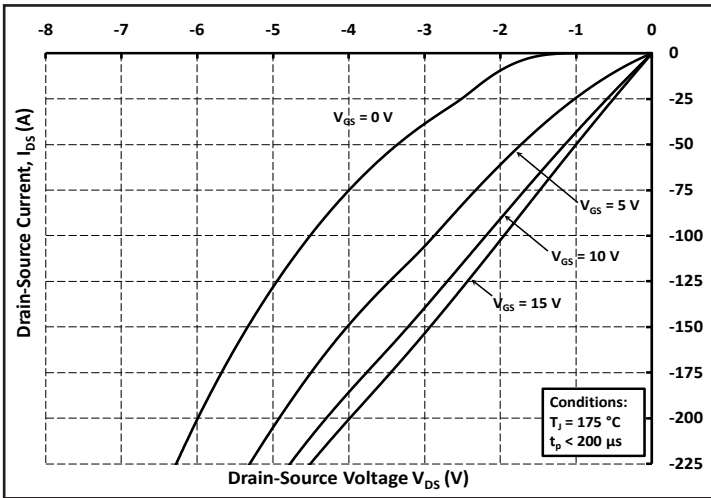


Figure 15. 3rd Quadrant Characteristic at 175 °C

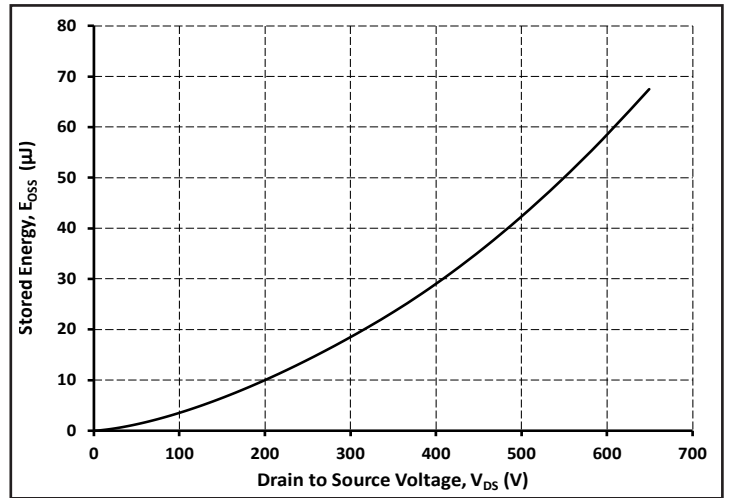


Figure 16. Output Capacitor Stored Energy

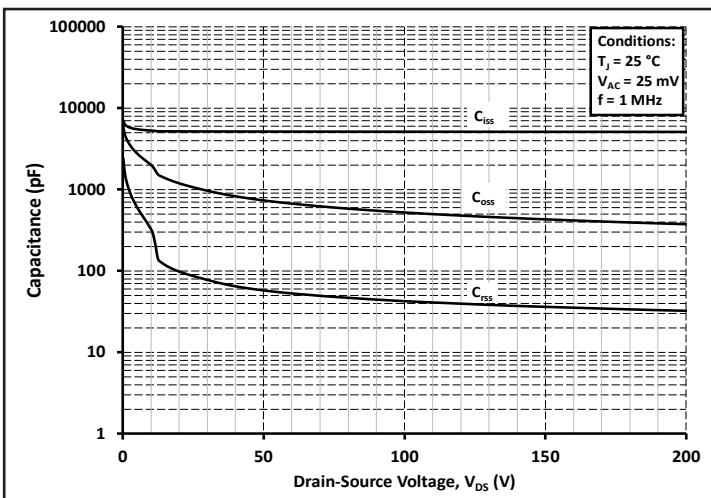


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

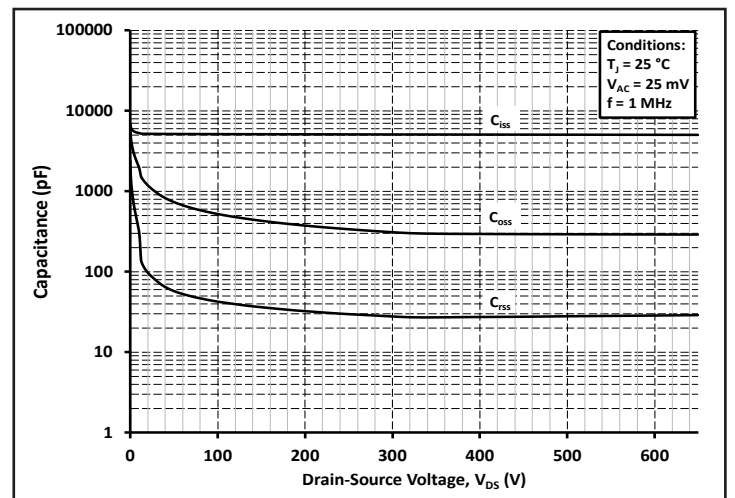


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)



Typical Performance

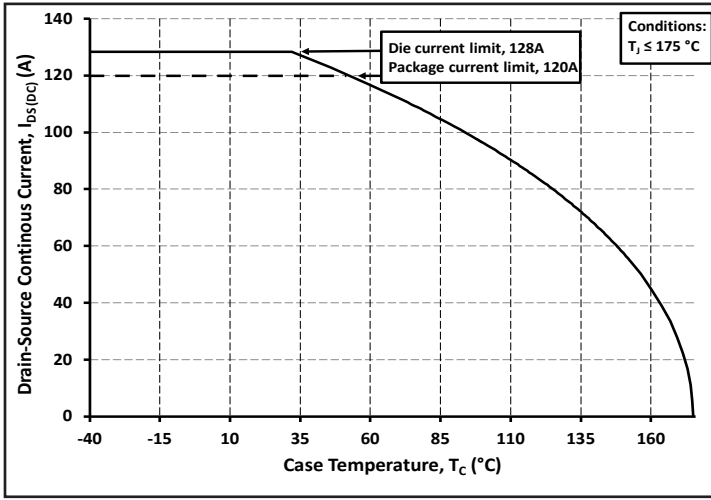


Figure 19. Continuous Drain Current Derating vs. Case Temperature

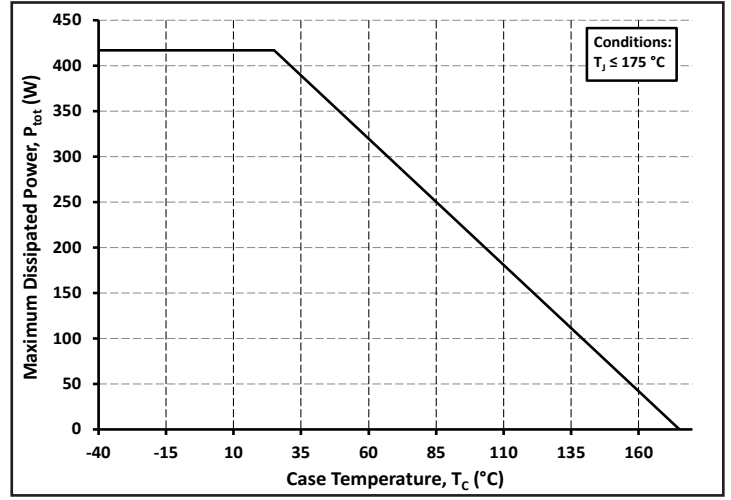


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

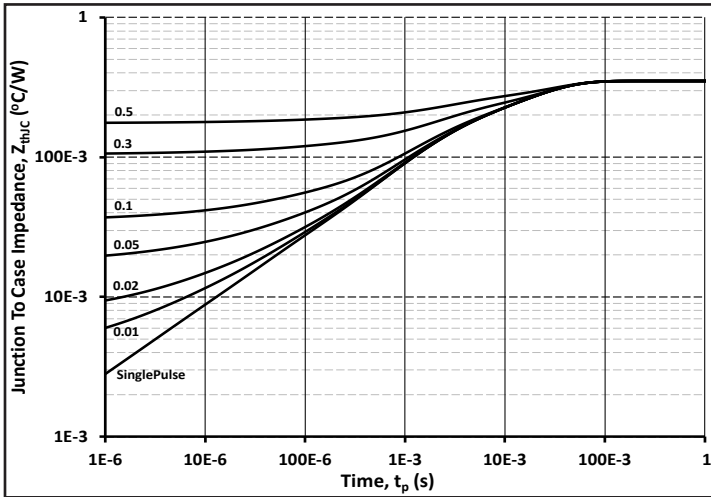


Figure 21. Transient Thermal Impedance (Junction - Case)

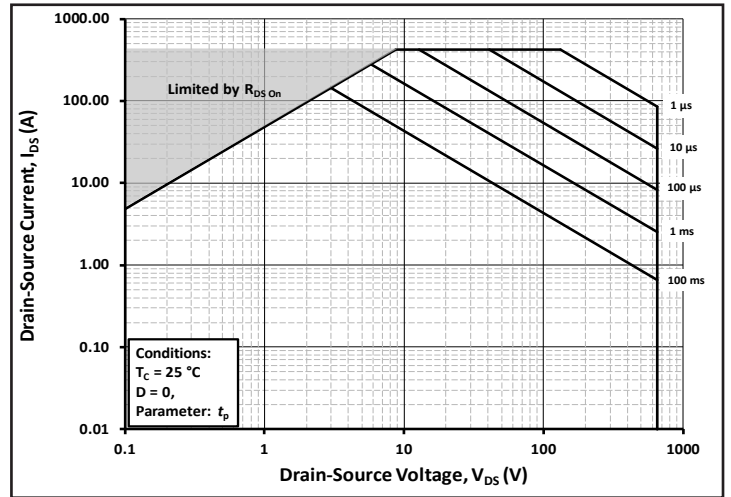


Figure 22. Safe Operating Area

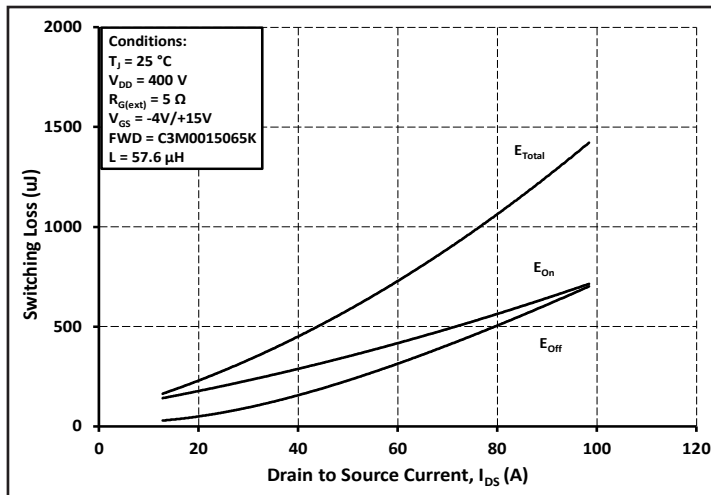


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 400V$)

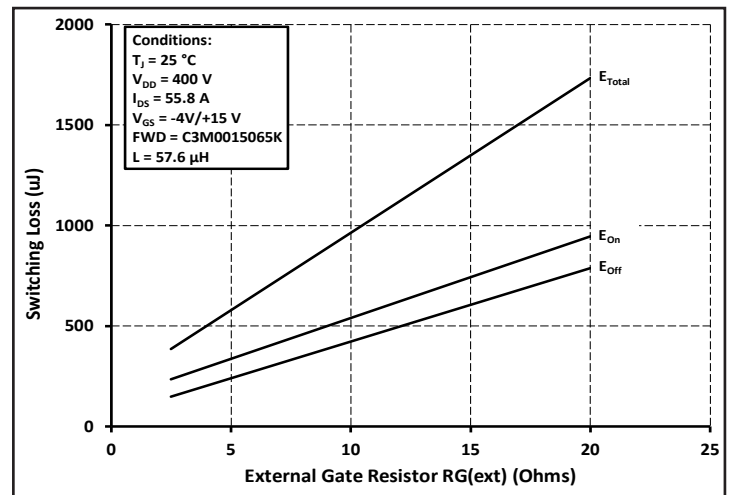


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$



Typical Performance

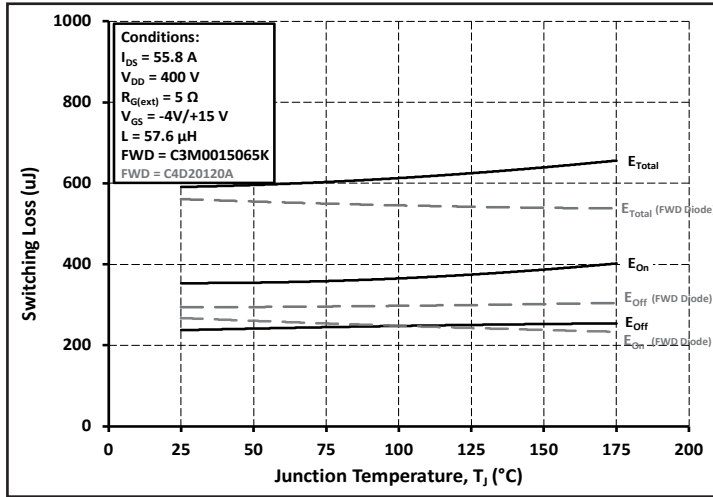


Figure 25. Clamped Inductive Switching Energy vs. Temperature

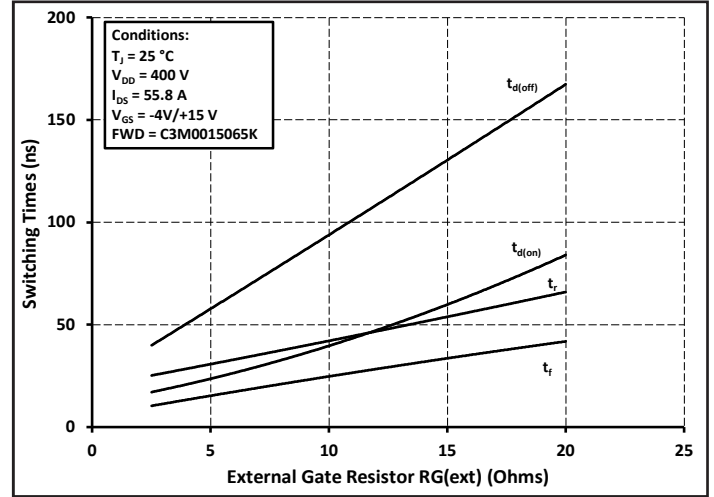


Figure 26. Switching Times vs. $R_{G(ext)}$



Test Circuit Schematic

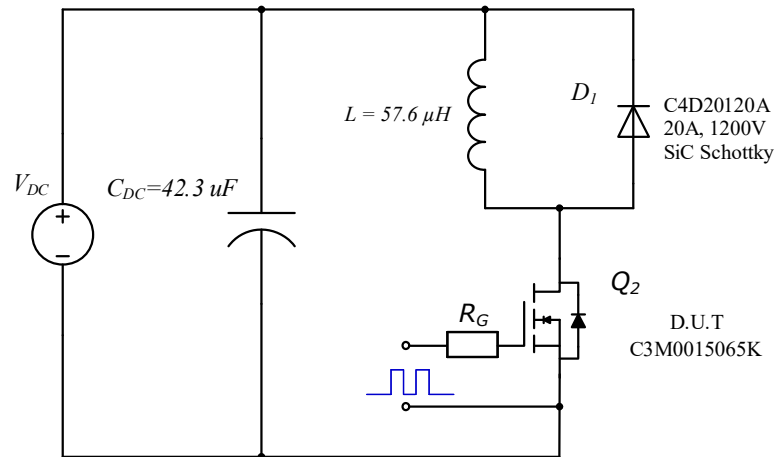


Figure 27. Clamped Inductive Switching Waveform Test Circuit

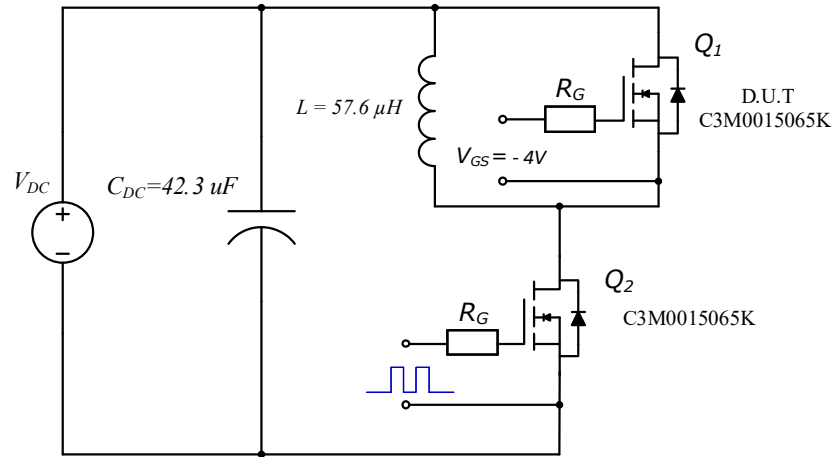
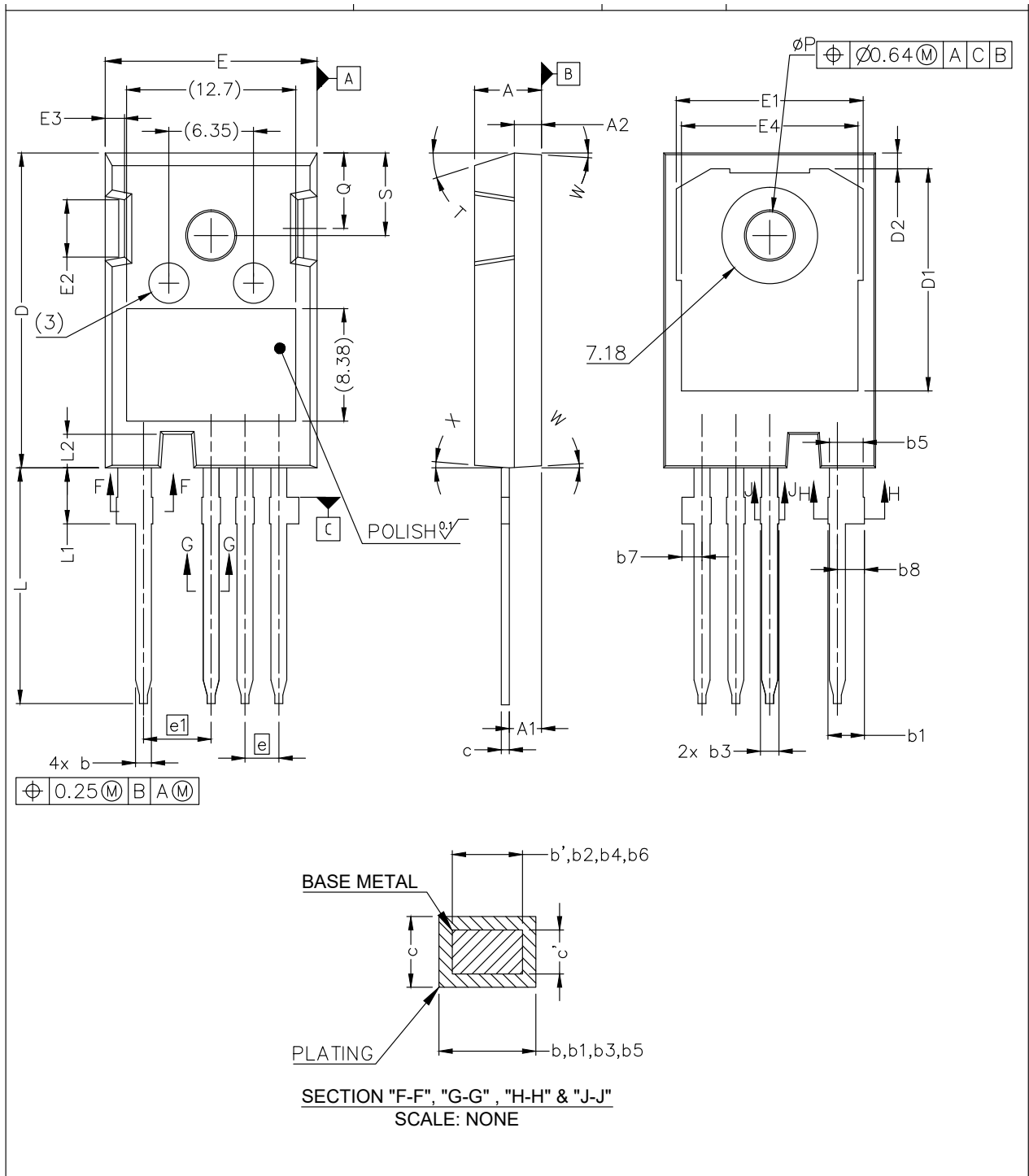


Figure 28. Body Diode Recovery Test Circuit



Package Dimensions

TO-247-4L



Package Dimensions

TO-247-4L

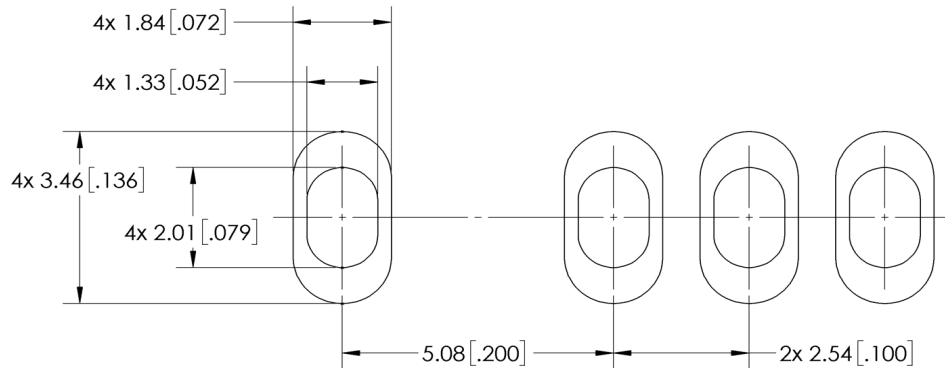
NOTE ;

1. ALL METAL SURFACES: TIN PLATED, EXCEPT AREA OF CUT .
2. DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. 'N' IS THE NUMBER OF TERMINAL POSITIONS.
5. DIMENSION DO NOT INCLUDE BURR OR MOLD FLASH.

| SYM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 4.83 | 5.21 |
| A1 | 2.29 | 2.54 |
| A2 | 1.91 | 2.16 |
| b' | 1.07 | 1.28 |
| b | 1.07 | 1.33 |
| b1 | 2.39 | 2.94 |
| b2 | 2.39 | 2.84 |
| b3 | 1.07 | 1.60 |
| b4 | 1.07 | 1.50 |
| b5 | 2.39 | 2.69 |
| b6 | 2.39 | 2.64 |
| b7 | 1.30 | 1.70 |
| b8 | 1.80 | 2.20 |

| | | |
|----|------------|-------|
| c' | 0.55 | 0.65 |
| c | 0.55 | 0.68 |
| D | 23.30 | 23.60 |
| D1 | 16.25 | 17.65 |
| D2 | 0.95 | 1.25 |
| E | 15.75 | 16.13 |
| E1 | 13.10 | 14.15 |
| E2 | 3.68 | 5.10 |
| E3 | 1.00 | 1.90 |
| E4 | 12.38 | 13.43 |
| e | 2.54 BSC | |
| e1 | 5.08 BSC | |
| N* | 4 | |
| L | 17.31 | 17.82 |
| L1 | 3.97 | 4.37 |
| L2 | 2.35 | 2.65 |
| øP | 3.51 | 3.65 |
| Q | 5.49 | 6.00 |
| S | 6.04 | 6.30 |
| T | 17.5° REF. | |
| W | 3.5° REF. | |
| X | 4° REF. | |

Recommended Solder Pad Layout





Notes

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For more information please contact:
4600 Silicon Drive Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfspeed.com/power