# 18 Output, 3.3V SDRAM Buffer for Desktop PCs with 4 DIMMs

## Features

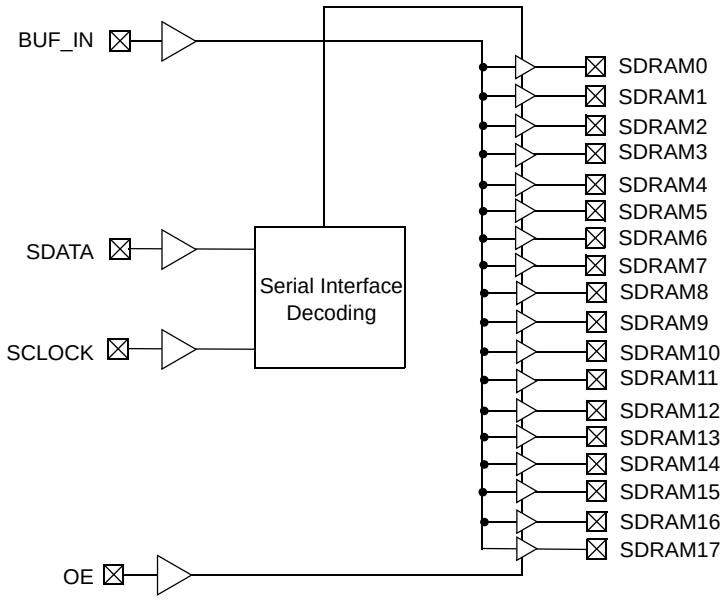
- **One input to 18 output buffer/driver**
- **Supports up to four SDRAM DIMMs**
- **Two additional outputs for feedback**
- **Serial interface for individual output control**
- **150ps typical output-output skew**
- **Up to 100 MHz operation**
- **Dedicated OE pin for testing**
- **Space-saving 48-pin SSOP package**
- **3.3V operation**

## Functional Description

The CY2318ANZ is a 3.3V buffer designed to distribute high-speed clocks in PC applications. The part has 18 outputs, 16 of which can be used to drive up to four SDRAM DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 100 MHz, thus making it compatible with Pentium II® processors. The CY2318ANZ can be used in conjunction with the CY2280, CY2281, CY2282 or similar clock synthesizer for a complete Pentium II motherboard solution.

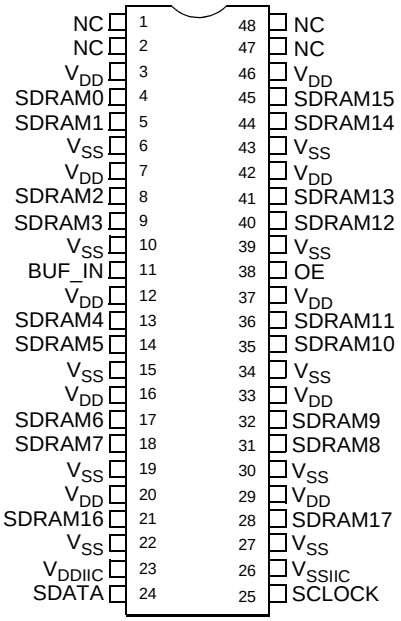
The CY2318ANZ also includes a serial interface which can enable or disable each output clock. On power-up, all output clocks are enabled (internal pull up). A separate Output Enable pin facilitates testing on ATE.

## Block Diagram




## Pin Configuration

**SSOP**
**Top View**



## Pin Summary

| Name | Pins | Description |
|---|---|---|
| $V_{DD}$ | 3, 7, 12, 16, 20, 29, 33, 37, 42, 46 | 3.3V Digital voltage supply |
| $V_{SS}$ | 6, 10, 15, 19, 22, 27, 30, 34, 39, 43 | Ground |
| $V_{DDIIC}$ | 23 | Serial interface voltage supply |
| $V_{SSIIC}$ | 26 | Ground for serial interface |
| BUF_IN | 11 | Input clock (5V Tolerant) |
| OE | 38 | Output Enable (active HIGH), Three-state outputs when low[1] |
| SDATA | 24 | Serial data input[1] |
| SCLK | 25 | Serial clock input[1] |
| SDRAM [0–3] | 4, 5, 8, 9 | SDRAM byte 0 clock outputs |
| SDRAM [4–7] | 13, 14, 17, 18 | SDRAM byte 1 clock outputs |
| SDRAM [8–11] | 31, 32, 35, 36 | SDRAM byte 2 clock outputs |
| SDRAM [12–15] | 40, 41, 44, 45 | SDRAM byte 3 clock outputs |
| SDRAM [16–17] | 21, 28 | SDRAM clock outputs usable for feedback |
| N/C | 1, 2, 47, 48 | Reserved for future modifications, do not connect in system |

**Note:**
1. Internal pull-up resistor to $V_{DD}$ (value > 100 kohms)

## Device Functionality

| OE | SDRAM [0–17] |
|---|---|
| 0 | Hi-Z |
| 1 | 1 x BUF_IN |

## Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  .
  .
  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to “0”.
- Serial interface address for the CY2318ANZ is:

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | ---- |

**Byte 0:SDRAM Active/Inactive Register**
**(1 = Active, 0 = Inactive), Default = Active**

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | 18 | SDRAM7 (Active/Inactive) |
| Bit 6 | 17 | SDRAM6 (Active/Inactive) |
| Bit 5 | 14 | SDRAM5 (Active/Inactive) |
| Bit 4 | 13 | SDRAM4 (Active/Inactive) |
| Bit 3 | 9 | SDRAM3 (Active/Inactive) |
| Bit 2 | 8 | SDRAM2 (Active/Inactive) |
| Bit 1 | 5 | SDRAM1 (Active/Inactive) |
| Bit 0 | 4 | SDRAM0 (Active/Inactive) |

**Byte 1: SDRAM Active/Inactive Register**
**(1 = Active, 0 = Inactive), Default = Active**

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | 45 | SDRAM15 (Active/Inactive) |
| Bit 6 | 44 | SDRAM14 (Active/Inactive) |
| Bit 5 | 41 | SDRAM13 (Active/Inactive) |
| Bit 4 | 40 | SDRAM12 (Active/Inactive) |
| Bit 3 | 36 | SDRAM11 (Active/Inactive) |
| Bit 2 | 35 | SDRAM10 (Active/Inactive) |
| Bit 1 | 32 | SDRAM9 (Active/Inactive) |
| Bit 0 | 31 | SDRAM8 (Active/Inactive) |

**Byte 2: SDRAM Active/Inactive Register**
**(1 = Active, 0 = Inactive), Default = Active**

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | 28 | SDRAM17 (Active/Inactive) |
| Bit 6 | 21 | SDRAM16 (Active/Inactive) |
| Bit 5 | -- | Reserved, drive to 0 |
| Bit 4 | -- | Reserved, drive to 0 |
| Bit 3 | -- | Reserved, drive to 0 |
| Bit 2 | -- | Reserved, drive to 0 |
| Bit 1 | -- | Reserved, drive to 0 |
| Bit 0 | -- | Reserved, drive to 0 |

## Maximum Ratings

Supply Voltage to Ground Potential .....–0.5 to +7.0V
DC Input Voltage (except BUF_IN) ..... –0.5V to $V_{DD}$ + 0.5
DC Input Voltage (BUF_IN)..... –0.5V to 7.0V

Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... +150°C
Static Discharge Voltage..... >2000V
(per MIL-STD-883, Method 3015)

## Operating Conditions

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$, $V_{DDIIC}$ | Supply Voltage | 3.135 | 3.465 | V |
| $T_A$ | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| $C_L$ | Load Capacitance | 20 | 30 | pF |
| $C_{IN}$ | Input Capacitance | | 7 | pF |
| $t_{PU}$ | Power-up time for all $V_{DD}$s to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 50 | ms |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage[2] | For all pins except serial interface pins | | 0.8 | V |
| $V_{ILiic}$ | Input LOW Voltage | For serial pins only | | 0.7 | V |
| $V_{IH}$ | Input HIGH Voltage[2] | | 2.0 | | V |
| $I_{IL}$ | Input LOW Current (BUF_IN input) | $V_{IN}$ = 0V | –10 | 10 | µA |
| $I_{IL}$ | Input LOW Current (Except BUF_IN Pin) | $V_{IN}$ = 0V | | 100 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{IN} = V_{DD}$ | –10 | 10 | µA |
| $V_{OL}$ | Output LOW Voltage[3] | $I_{OL}$ = 25 mA | | 0.4 | V |
| $V_{OH}$ | Output HIGH Voltage[3] | $I_{OH}$ = –36 mA | 2.4 | | V |
| $I_{DD}$ | Supply Current[3] | Unloaded outputs, 100 MHz | | 200 | mA |
| $I_{DD}$ | Supply Current | Loaded outputs, 100 MHz | | 360 | mA |
| $I_{DD}$ | Supply Current[3] | Unloaded outputs, 66.67 MHz | | 150 | mA |
| $I_{DD}$ | Supply Current | Loaded outputs, 66.67 MHz | | 230 | mA |
| $I_{DDS}$ | Supply Current | BUF_IN = $V_{DD}$ or $V_{SS}$, all other inputs at $V_{DD}$ | | 500 | µA |

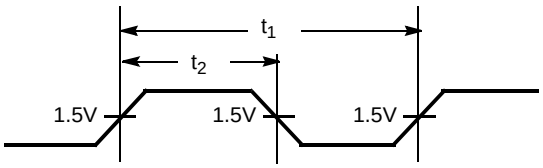
**Notes:**
2. BUF_IN input has a threshold voltage of $V_{DD}/2$.
3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Switching Characteristics[4]

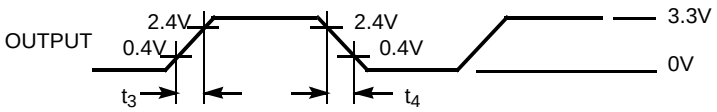
| Parameter | Name | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | Maximum Operating Frequency | | | | 100 | MHz |
| | Duty Cycle[3, 5] = $t_2 \div t_1$ | Measured at 1.5V | 45.0 | 50.0 | 55.0 | % |
| $t_3$ | Rising Edge Rate[3] | Measured between 0.4V and 2.4V | 0.9 | 1.5 | 4.0 | V/ns |
| $t_4$ | Falling Edge Rate[3] | Measured between 2.4V and 0.4V | 0.9 | 1.5 | 4.0 | V/ns |
| $t_5$ | Output to Output Skew[3] | All outputs equally loaded | | 150 | 250 | ps |
| $t_6$ | SDRAM Buffer LH Prop. Delay[3] | Input edge greater than 1 V/ns | 1.0 | 3.5 | 5.0 | ns |
| $t_7$ | SDRAM Buffer HL Prop. Delay[3] | Input edge greater than 1 V/ns | 1.0 | 3.5 | 5.0 | ns |
| $t_8$ | SDRAM Buffer Enable Delay[3] | Input edge greater than 1 V/ns | 1.0 | 5 | 12 | ns |
| $t_9$ | SDRAM Buffer Disable Delay[3] | Input edge greater than 1 V/ns | 1.0 | 20 | 30 | ns |

## Switching Waveforms

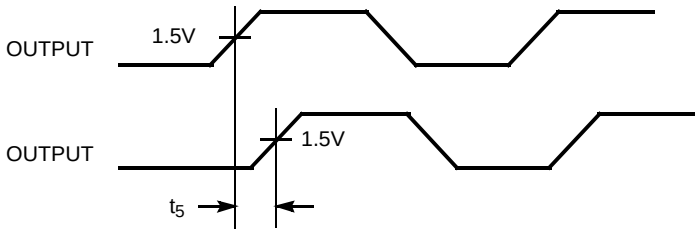
### Duty Cycle Timing




### All Outputs Rise/Fall Time



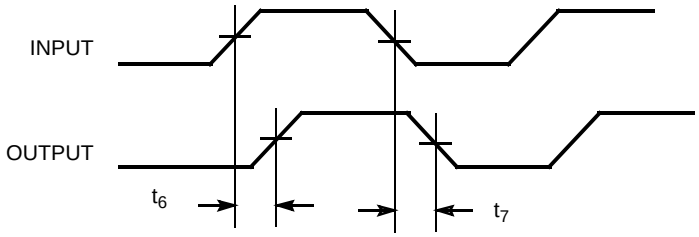

### Output-Output Skew



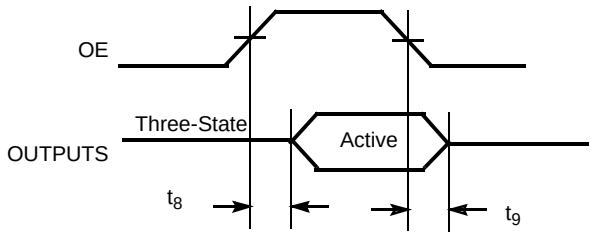

**Notes:**
4. All parameters specified with loaded outputs.
5. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1 V/ns.

## Switching Waveforms (continued)

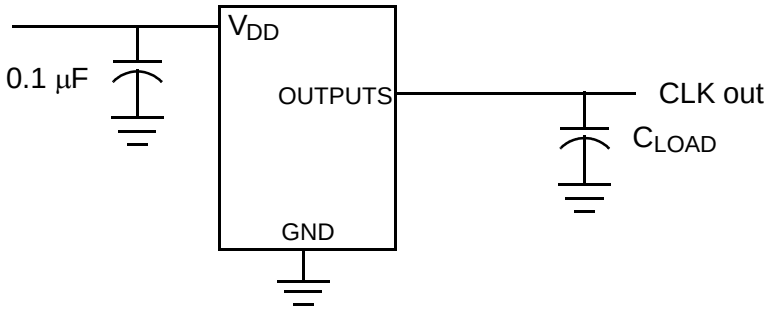
### SDRAM Buffer LH and HL Propagation Delay



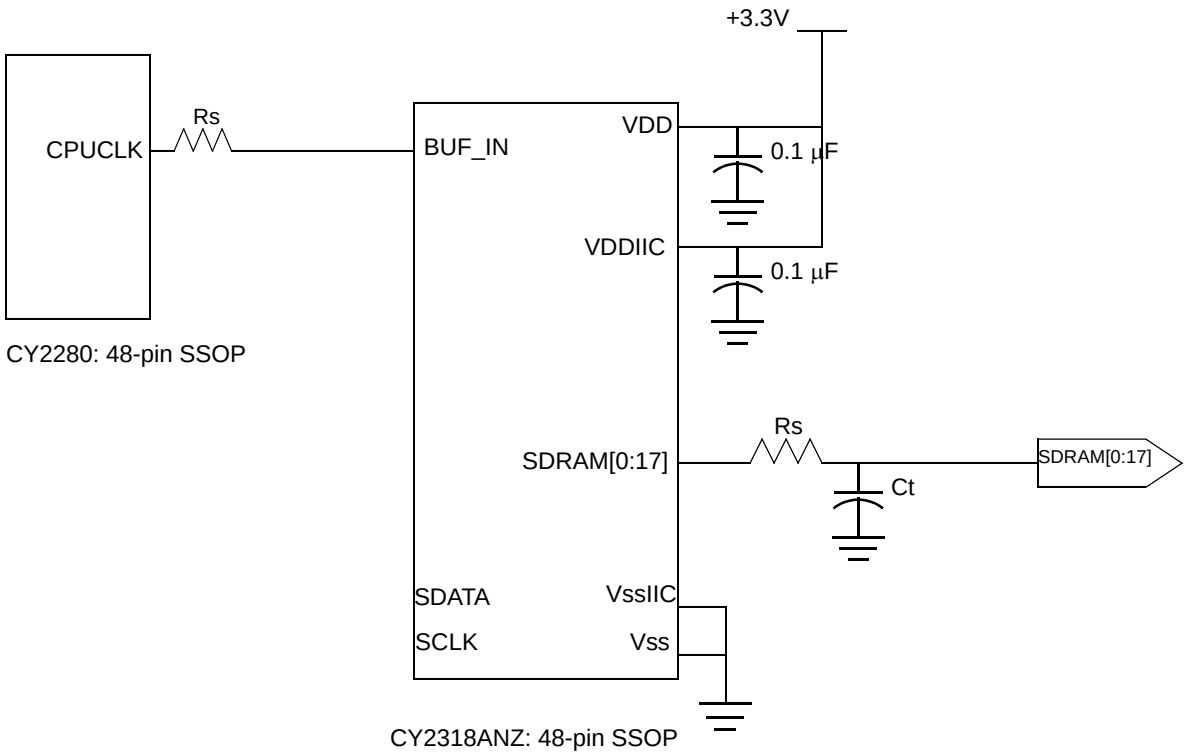

### SDRAM Buffer Enable and Disable Times




### Test Circuit



## Application Circuit



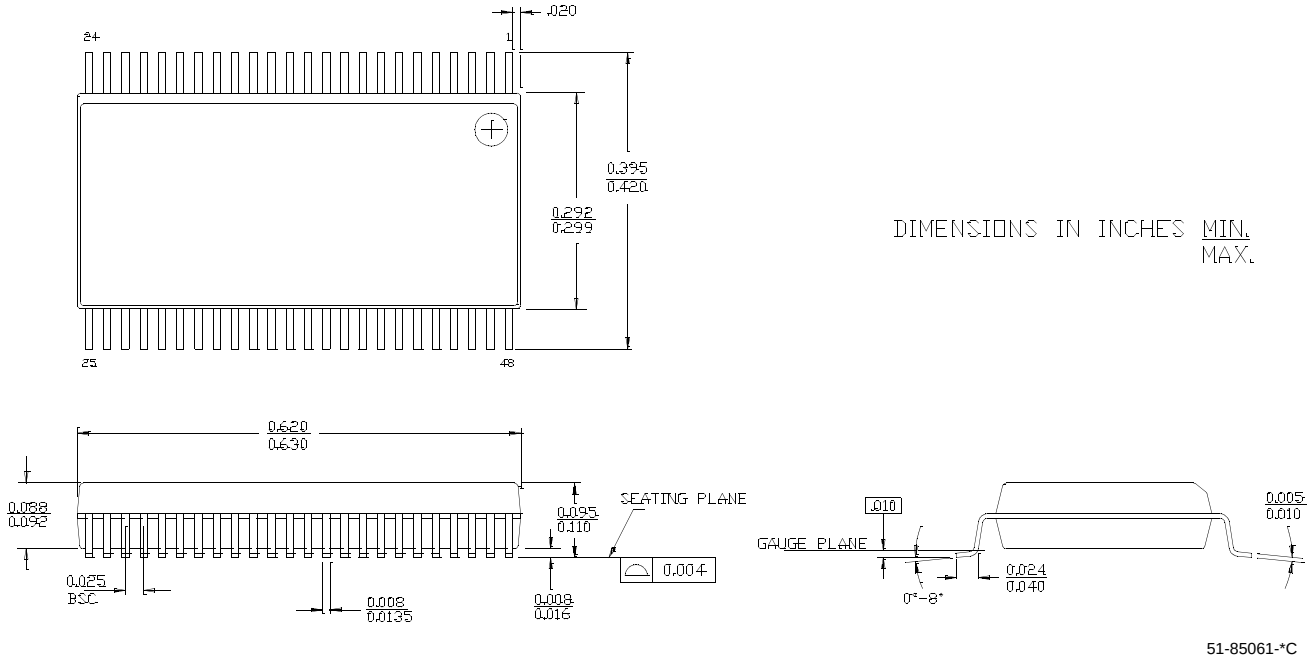

Rs = Series termination resistor
Ct = Optional cap to reduce EMI

## Ordering Information

| Ordering Code | Package Type | Operating Range |
|---|---|---|
| CY2318ANZPVC–11 | 48-pin SSOP | Commercial |
| CY2318ANZPVC–11T | 48-pin SSOP - Tape and Reel | Commercial |
| **Lead-free** | | |
| CY2318ANZPVXC–11 | 48-pin SSOP | Commercial |
| CY2318ANZPVXC–11T | 48-pin SSOP- Tape and Reel | Commercial |

## Package Diagram

**48-Lead Shrunk Small Outline Package O48**

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## Document History Page

| Document Title: CY2318ANZ 18 Output, 3.3V SDRAM Buffer for Desktop PCs with 4 DIMMs<br>Document Number: 38-07181 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 111857 | 12/09/01 | DSG | Change from Spec number: 38-00771 to 38-07181 |
| *A | 121833 | 12/14/02 | RBI | Power up requirements added to Operating Conditions Information |
| *B | 310577 | See ECN | RGL | Added Tape and Reel option<br>Added Lead-free Devices |
| *C | 399949 | See ECN | RGL | Minor Change: Corrected the ordering code for the lead-free devices to match the devmaster |