

MC74AC259, MC74ACT259

8-Bit Addressable Latch

The MC74AC259/74ACT259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable. It is functionally identical to the ALS259 8-bit addressable latch.

- Serial-to-Parallel Conversion
- Eight Bits of Storage with Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear
- These are Pb-Free Devices

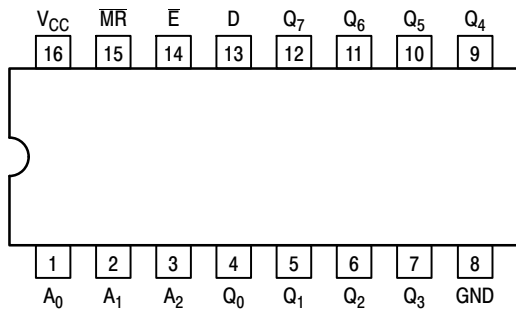


Figure 1. Pinout: 16-Lead Packages Conductors (Top View)

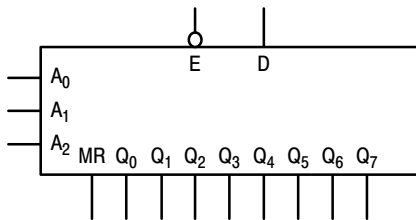


Figure 2. Logic Symbol

MODE SELECT TABLE

E	MR	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

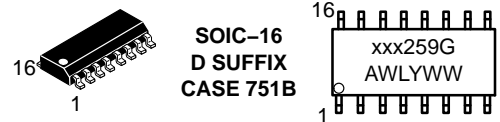
H = HIGH Voltage Level
L = LOW Voltage Level



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MARKING DIAGRAM



xxx = AC or ACT
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

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MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs						Outputs							
	\overline{MR}	\overline{E}	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (Active HIGH Decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Store (Do Nothing)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable Latch	H	L	d	L	L	L	Q = d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀	Q = d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	Q = d	q ₃	q ₄	q ₅	q ₆	q ₇
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
H	L	d	H	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q = d	

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

d = HIGH or LOW Data one setup time prior to the LOW-to-HIGH Enable transition

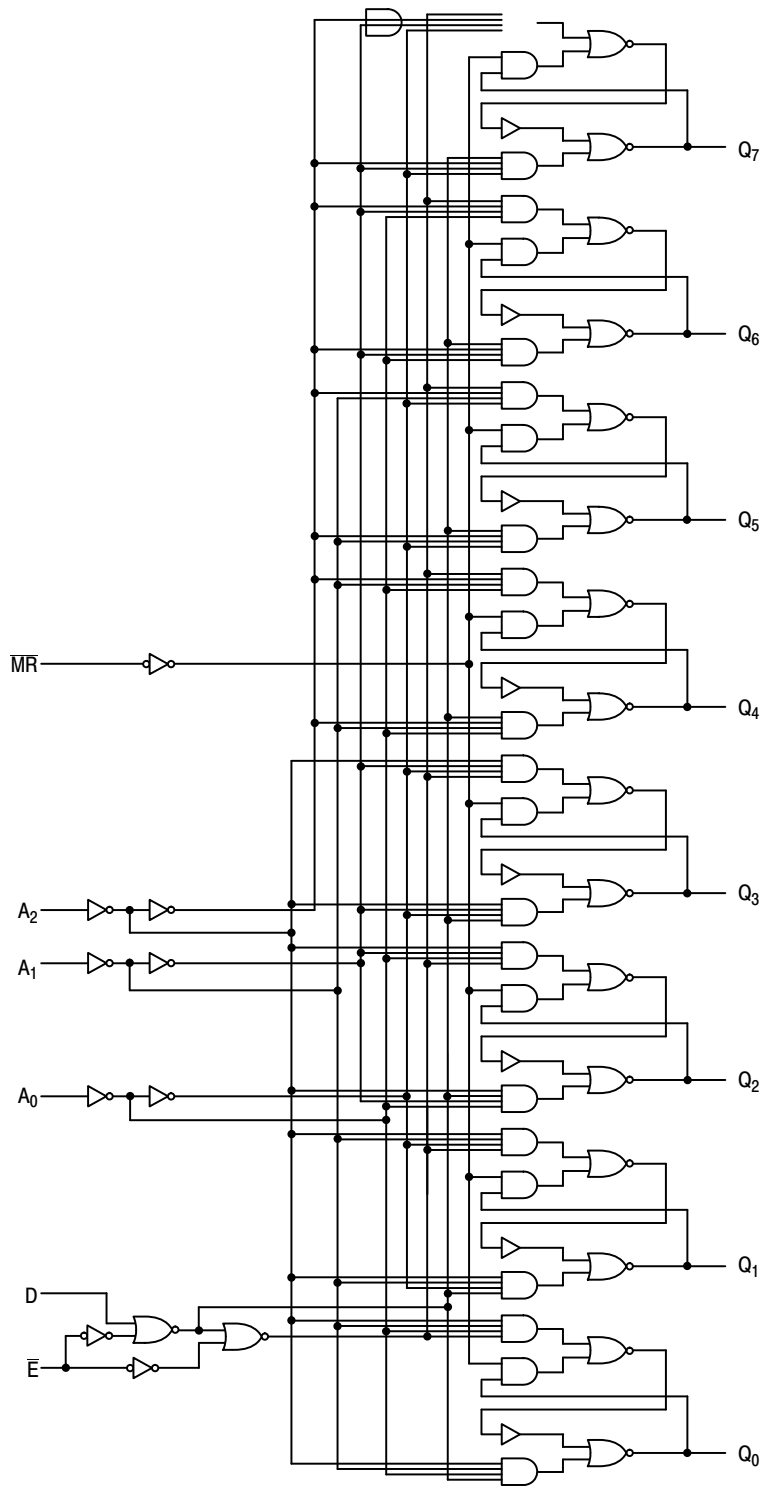
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

FUNCTIONAL DESCRIPTION

The MC74AC259/74ACT259 has four modes of operation as shown in the Mode Selection Table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states in the memory mode. All latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the MC74AC/ACT259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The Mode Select Function Table summarizes the operations of the MC74AC/ACT259.

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NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V	
V _I	DC Input Voltage	-0.5 ≤ V _{CC} +0.5	V	
V _O	DC Output Voltage (Note 1)	-0.5 ≤ V _{CC} +0.5	V	
I _{IK}	DC Input Diode Current	±20	mA	
I _{OK}	DC Output Diode Current	±50	mA	
I _O	DC Output Sink/Source Current	±50	mA	
I _{CC}	DC Supply Current per Output Pin	±50	mA	
I _{GND}	DC Ground Current per Output Pin	±50	mA	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
T _L	Lead temperature, 1 mm from Case for 10 Seconds	260	°C	
T _J	Junction temperature under Bias	+150	°C	
θ _{JA}	Thermal Resistance (Note 2)	69.1	°C/W	
P _D	Power Dissipation in Still Air at 65°C (Note 3)	500	mW	
MSL	Moisture Sensitivity	Level 1		
F _R	Flammability Rating	Oxygen Index: 30% – 35% UL 94 V-0 @ 0.125 in		
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 4) Machine Model (Note 5) Charged Device Model (Note 6)	> 2000 > 200 > 1000	V
I _{Latch-Up}	Latch-Up Performance	Above V _{CC} and Below GND at 85°C (Note 7)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51-7.
3. 500 mW at 65°C; derate to 300 mW by 10 mW/°C from 65°C to 85°C.
4. Tested to EIA/JESD22-A114-A.
5. Tested to EIA/JESD22-A115-A.
6. Tested to JESD22-C101-A.
7. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)	0	-	V _{CC}	V	
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	-	150	-	ns/V
		V _{CC} @ 4.5 V	-	40	-	
		V _{CC} @ 5.5 V	-	25	-	
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	-	10	-	ns/V
		V _{CC} @ 5.5 V	-	8.0	-	
T _A	Operating Ambient Temperature Range	-40	25	85	°C	
I _{OH}	Output Current – High	-	-	-24	mA	
I _{OL}	Output Current – Low	-	-	24	mA	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I _{OUT} = -50 μA
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0	-	2.56	2.46		V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} = -24 mA -24 mA
		4.5	-	3.86	3.76			
		5.5	-	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0	-	0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} = 24 mA 24 mA
		4.5	-	0.36	0.44			
		5.5	-	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0		μA	V _I = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	-	-	-75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to Q _n	3.3 5.0	2.0 2.0	9.0 6.5	14.5 10.0	1.5 1.5	17.0 11.5	ns	3-5
t _{PHL}	Propagation Delay D _n to Q _n	3.3 5.0	2.0 2.0	9.0 6.0	13.5 9.5	1.5 1.5	16.0 11.0	ns	3-5
t _{PLH}	Propagation Delay E to Q _n	3.3 5.0	2.0 2.0	10.5 7.0	15.0 10.5	1.5 1.5	17.5 12.5	ns	3-6
t _{PHL}	Propagation Delay E to Q _n	3.3 5.0	2.0 2.0	8.0 7.5	12.5 9.0	1.5 1.5	15.0 11.0	ns	3-6
t _{PLH}	Propagation Delay Address to Q _n	3.3 5.0	2.0 2.0	12.0 8.0	19.0 13.0	1.5 1.5	22.5 15.5	ns	3-6
t _{PHL}	Propagation Delay Address to Q _n	3.3 5.0	2.0 2.0	10.0 7.0	16.0 11.0	1.5 1.5	19.0 13.0	ns	3-6
t _{PHL}	Propagation Delay \overline{MR} to Q	3.3 5.0	2.0 2.0	8.0 6.0	12.0 9.0	1.5 1.5	13.5 10.0	ns	3-7

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to \overline{E}	3.3 5.0	– –	3.5 2.5	4.5 3.5		ns	3-9
t _h	Hold Time, HIGH or LOW D _n to \overline{E}	3.3 5.0	– –	2.5 2.0	2.5 2.0		ns	3-9
t _s	Setup Time Address to \overline{E}	3.3 5.0	– –	7.0 4.0	9.0 6.0		ns	3-6
t _h	Hold Time Address to \overline{E}	3.3 5.0	– –	2.0 2.0	2.0 2.0		ns	3-6
t _w	Minimum Pulse Width \overline{MR}	3.3 5.0	– –	6.0 5.5	6.5 6.0		ns	3-6
t _w	Minimum Pulse Width \overline{E}	3.3 5.0	– –	6.5 5.5	7.0 6.0		ns	3-6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4		V	I _{OUT} = -50 μA
		5.5	5.49	5.4	5.4			
		4.5	-	3.86	3.76		V	*V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} -24 mA
		5.5	-	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1		V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1			
		4.5	-	0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
		5.5	-	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0		μA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6	-	1.5		mA	V _I = V _{CC} - 2.1 V
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	-	-	-75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to Q _n	5.0	2.0	6.5	11.0	1.5	12.5	ns	3-5
t _{PHL}	Propagation Delay D _n or Q _n	5.0	2.0	7.0	10.5	1.5	12.0	ns	3-5
t _{PLH}	Propagation Delay E̅ to Q _n	5.0	2.0	10.5	14.0	1.5	16.5	ns	3-6
t _{PHL}	Propagation Delay E̅ or Q _n	5.0	2.0	9.0	12.0	1.5	14.0	ns	3-6
t _{PLH}	Propagation Delay Address to Q _n	5.0	2.0	8.0	11.5	1.5	13.5	ns	3-6
t _{PHL}	Propagation Delay Address to Q _n	5.0	2.0	6.0	10.0	1.5	12.0	ns	3-6
t _{PHL}	Propagation Delay MR to Q	5.0	2.0		10.0	1.5	11.0	ns	3-7

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to \bar{E}	5.0	-	3.0	4.0	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to \bar{E}	5.0	-	2.5	2.5	ns	3-9	
t _s	Setup Time Address to \bar{E}	5.0	-	4.5	6.5	ns	3-6	
t _h	Hold Time Address to \bar{E}	5.0	-	2.5	2.5	ns	3-6	
t _w	Minimum Pulse Width $\bar{M}\bar{R}$	5.0	-	7.0	7.5	ns	3-6	
t _w	Minimum Pulse Width \bar{E}	5.0	-	7.0	7.5	ns	3-6	

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50.0	pF	V _{CC} = 5.0 V

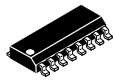
ORDERING INFORMATION

Part Number	Package	Shipping†
MC74AC259DG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74AC259DR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC74ACT259DG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74ACT259DR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

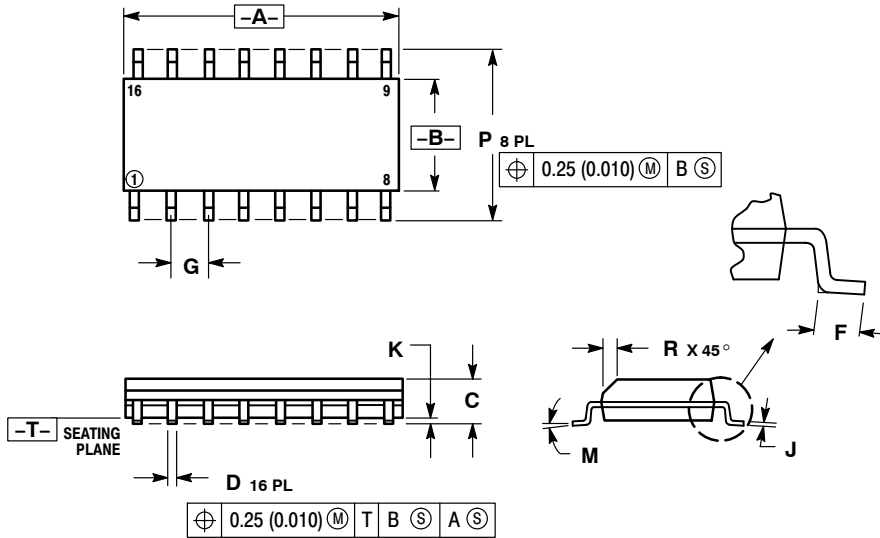
ON Semiconductor®



SCALE 1:1

SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



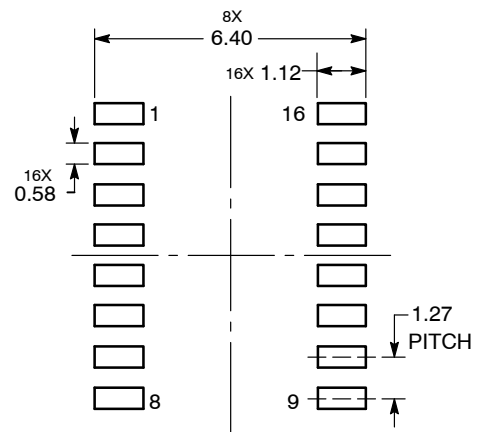
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- | | | | |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p> | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p> | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> | |

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