

PCN Number:	20180509001.1		PCN Date:	May 18, 2018	
Title:	LBC7 change total PO thickness from 24kA to 39kA				
Customer Contact:	PCN Manager		Dept:	Quality Services	
Proposed 1st Ship Date:	Aug 18, 2018	Estimated Sample Availability:	Date provided at sample request.		
Change Type:					
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Assembly Process	<input type="checkbox"/>	Assembly Materials
<input type="checkbox"/>	Design	<input type="checkbox"/>	Electrical Specification	<input type="checkbox"/>	Mechanical Specification
<input type="checkbox"/>	Test Site	<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>	Wafer Bump Site	<input type="checkbox"/>	Wafer Bump Material	<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>	Wafer Fab Site	<input type="checkbox"/>	Wafer Fab Materials	<input checked="" type="checkbox"/>	Wafer Fab Process
	<input type="checkbox"/>	Part number change			
PCN Details					
Description of Change:					
This change notification is to announce a total PO Thickness change from 24kA to 39kA by increasing the 2 nd Oxide Teos thickness from 3kA to 18kA on the LBC7 process node for the selected devices listed in the "Product Affected" section.					
Change From		Change To			
13kA HDP Oxide + 3kA Teos Oxide + 8kA Nitride passivation		13kA HDP Oxide + 18kA Teos Oxide + 8kA Nitride passivation			
Qual details are provided in the Qual Data Section.					
Reason for Change:					
Continuity of supply.					
Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):					
None					
Changes to product identification resulting from this PCN:					
None					
Product Affected:					
TPS53605DSQT	TPS562208DDCT	TPS563208DDCR	TPS7A9101DSKT		
TPS562201DDCR	TPS563201DDCR	TPS7A9001DSKR	TPS7A9201DSKR		
TPS562201DDCT	TPS563201DDCT	TPS7A9001DSKT	TPS7A9201DSKT		
TPS562208DDCR	TPS563201EDRLT	TPS7A9101DSKR			

Qualification Report

LBC7 - Thick TEOS at PO 2nd OX DEP

Approve Date 9-April-2018

Product Attributes

Attributes	Qual Device: TPS563201DDCR
Assembly Site	JCET
Package Family	SOT-23-T
Wafer Fab Supplier	RFAB
Wafer Process	LBC7
Flammability Rating	UL 94 V-0

- Qual Devices qualified at LEVEL1-NACG: Devices TPS563201DDCR

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	Test Name / Condition	Duration	Qual Device: TPS563201DDCR
HAST	Biased HAST, 130C/85%RH	192 Hours	3/231/0
HTSL	High Temp. Storage Bake, 170C	420 Hours	3/231/0
MQ	Manufacturability (Assembly)	(per mfg. Site specification)	3/Pass
TC	Temperature Cycle, -65/150C	750 Cycles	3/231/0

- Preconditioning was performed for Autodave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

- The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

- The following are equivalent HTSL options based on an activation energy of 0.7eV: 150C/1k Hours, and 170C/420 Hours

- The following are equivalent Temp Cycle options per JESD47: -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

Green/Pb-free Status:

Qualified Pb-Free (SMT) and Green

For questions regarding this notice, e-mails can be sent to the regional contacts shown below, or you can contact your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com