Timing Fabric for Communications Equipment

Integrated Device Technology

CLOCKS AND TIMING | INTERFACE AND CONNECTIVITY | MEMORY AND LOGIC | POWER MANAGEMENT | RF PRODUCTS

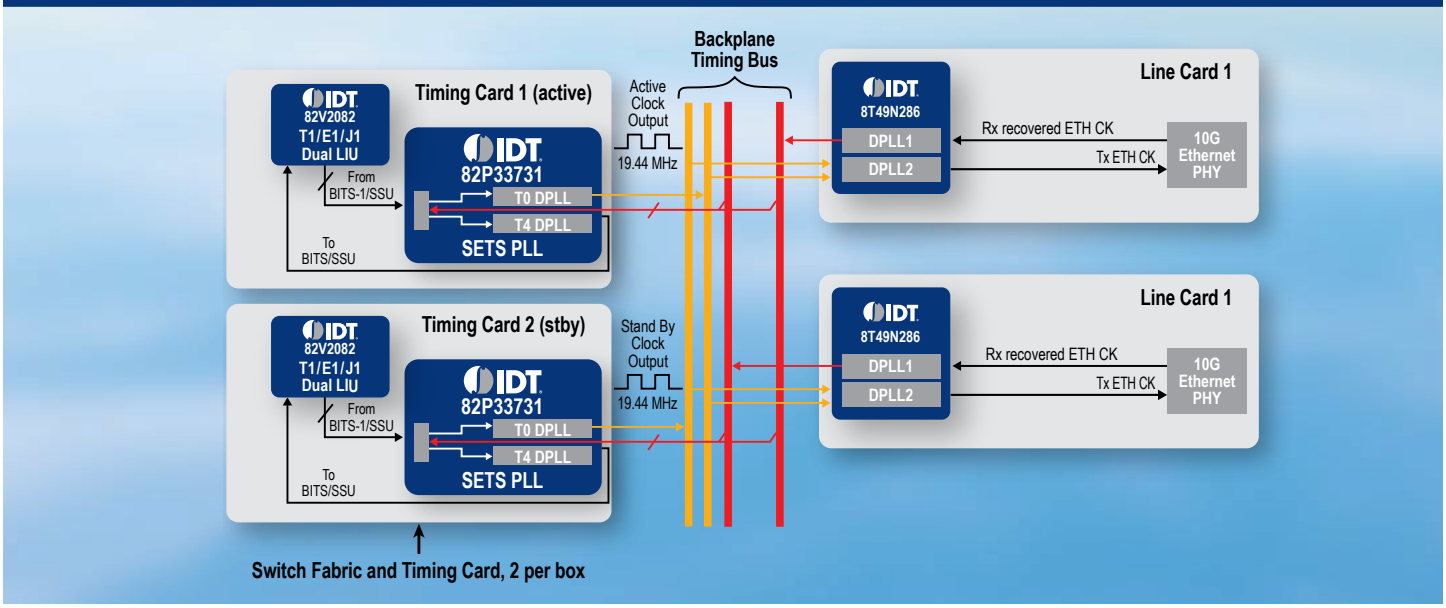

Figure 1 - Timing Fabric Architecture - Timing Cards and Line Cards

IDT LINE CARD SOLUTIONS:

Line Card PLL Features

- Dual PLL chip: one can be used for the transmit path and the other for the receive path
- Programmable DPLL bandwidth
- Supports automatic hitless reference switching
- Generates output clocks for Synchronous Ethernet, SONET, SDH, BITS, GPS, 3G and GSM components
- Available in QFN, lead-free packages

Jitter Attenuator Features

- FemtoClock® product is a frequency multiplier and jitter attenuator component that generates low jitter Ethernet clocks and can easily meet 10 Gigabit Ethernet requirements
- Optimized for 10G Ethernet jitter attenuation
- Attenuates the phase jitter of the input clock by using a low-cost pullable fundamental mode VCXO crystal
- Available in QFN lead-free packages

IDT TIMING CARD SOLUTIONS

IDT SETS PLL Features

- Up to 14 total inputs and 14 outputs
- IEEE 1588 Support (External DCO Control)
- 2 independent DPLL + APLL paths
  - T0 path for node timing synchronization
  - T4 path for equipment synchronization
- Frequency Range: 1 Hz to 650 MHz
- Phase noise <1 ps RMS (12 kHz to 20 MHz)

ARCHITECTURE OVERVIEW

Communication equipment requires synchronization to transport multiple services (voice, data and video) over Carrier networks. The timing fabric, as illustrated in *Figure 1* and *Figure 2,* enables equipment such as routers, multi-service switching platforms, PON (Passive Optical Network) and DSLAM (Digital Subscriber Line Access Multiplexer), to meet the stringent synchronization requirements of communication networks.

The architecture in *Figure 1* segments the timing fabric into 2 major elements: timing cards and line cards. On the timing cards, the SETS PLLs are primarily responsible for compliance with synchronization standards. The T1/E1 LIUs receive external BITS/SSU references for the T0 DPLLs which generate standards compliant synchronous clocks and distribute them to the backplane for the line cards. Recovered clocks from the line card PHYs are used as references by the T4 DPLLs which rate convert them for the T1/E1 LIU transmitters that provide line references to the external BITS/SSU. On the line cards DPLLs select a backplane reference from one of the timing cards, the reference is rate converted and jitter attenuated to meet the needs of the specific PHYs used on these cards. Depending on the number of PHY reference clocks required on each line card a discrete fan-out buffer may also be needed. Recovered clocks from line card PHYs are rate converted to a backplane frequency (8 kHz, 19.44 MHz, or 25 MHz) and sent to the backplane for the T4 DPLLs on the timing cards.

The architecture in *Figure 2* has the timing fabric in one up-link transmission card. Both the traditional timing card and line card functionality are combined into one card. The recovered clock from the PHY is sent to the SETS PLL for filtering, frequency translation and generation of backplane clocks. The clock generated by the SETS PLL used as a transmitting clock for the PHY + Framer.

As the only supplier with all of the different timing components to provide complete solutions, IDT is uniquely positioned to meet the needs of communication equipment suppliers and offer compelling solutions for all timing fabric architectures.

- Standards compliant SETS PLLs (EEC, PEC-S-F*, SEC, ST3/SMC [ITU-T G.8263, G.8262, G.813 & Telcordia GR-253-CORE, GR-1244-CORE])
- Standards compliant SMU PLLs (independent SETS PLL plus T-BC, T-TSC [ITU-T G.8273.2] PLL)
- T1/E1 Dual LIUs
- Line card PLLs
- Jitter attenuators and frequency translators
- Differential fanout buffers with low additive RMS phase jitter
- Backplane interface / translators (as needed)

** With supporting 1588 filtering algorithm software*

IDT T1/E1 LIU Features

- Dual and Single channel LIU devices available
- Supports Hitless Protection Switching for 1+1 protection without external relays
- Receiver sensitivity exceeds -36 db @ 772 kHz and -43 dB @ 1024 kHz
- Programmable T1/E1/J1 switchability allows one bill of material for any line condition
- Loss of signal (LOS) and Alarm Indication Signal (AIS) detection
- JTAG interface
- Available in TQFG or FPBGA lead-free packages

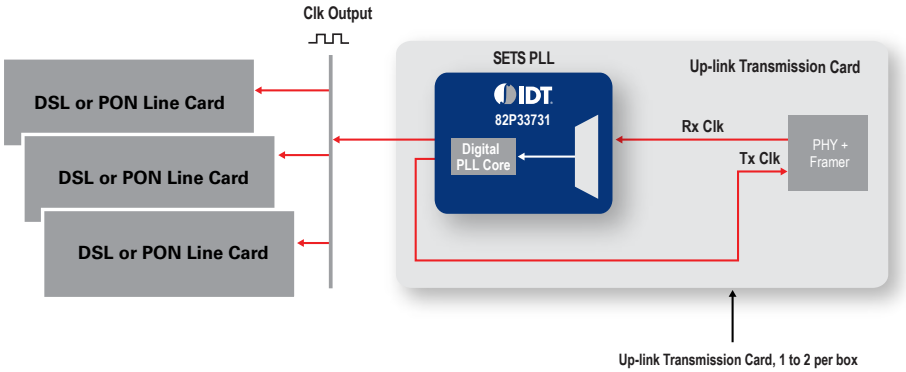

Figure 2 - Timing Fabric Architecture (Up-link Transmission Card)

Line Card Components

Part Number	Product Type	Outputs & Types	Output Frequencies (MHz)	Inputs & Type	Phase Jitter Typ RMS (ps)	Pkg. Dimensions
8T49N241	FemtoClock® NG Universal Frequency Translator	4 HCSL, LVCMOS, LVDS, LVPECL"	0.008 to 1000	2 HCSL, LVCMOS, LVDS, LVHSTL, LVPECL, LVTTL	0.35	6.0 x 6.0 x 0.9
8T49N242	FemtoClock NG Universal Frequency Translator	4 HCSL, LVCMOS, LVDS, LVPECL	0.008 to 1000	2 HCSL, LVCMOS, LVDS, LVHSTL, LVPECL, LVTTL"	0.35	6.0 x 6.0 x 0.9
8T49N285	FemtoClock NG Universal Frequency Translator (2-in/1-PLL/8-out)	8 HCSL, LVCMOS, LVDS, LVPECL	0.008 to 1000	2 HCSL, LVCMOS, LVDS, LVHSTL, LVPECL	0.28	8.0 x 8.0 x 0.85
8T49N286	FemtoClock NG Universal Frequency Translator (4-in/2-PLL/8-out)	8 HCSL, LVCMOS, LVDS, LVPECL	0.008 to 1000	4 HCSL, LVCMOS, LVDS, LVHSTL, LVPECL, LVTTL	0.28	10.0 x 10.0 x 1
8T49N287	FemtoClock NG Universal Frequency Translator (2-in/2-PLL/8-out)	8 HCSL, LVCMOS, LVDS, LVPECL	0.008 to 1000	2 HCSL, LVCMOS, LVDS, LVHSTL, LVPECL, LVTTL	0.28	8.0 x 8.0 x 0.85
8V89308i	Jitter Attenuator & FemtoClock Multiplier	2 LVPECL	25.0 to 156.25	1 LVDS, LVPECL	0.223	5.0 x 5.0 x 1

Timing Card/Up-link Transmission Card Component

Part Number	Product Type	Clock Support	Channels (#)	Inputs (#)	Diff. Inputs	Input Freq. Range Type	Output Freq. Range Type	Phase Jitter Typ RMS (ps)	Outputs (#)	Diff. Outputs
82P33714	Synchronous Equipment Timing Source for Synchronous Ethernet	G.813 (SEC), G.8262 (EEC), GR-253-CORE (SONET ST3/SMC), GR-1244-CORE (ST3/ ST4/ST4E)	2	6	4	1 Hz to 650 MHz	1 Hz to 650 MHz	0.56	12	4
82P33731	Synchronous Equipment Timing Source for 10G to 40G Synchronous Ethernet	G.813 (SEC), G.8262 (EEC), GR-253-CORE (SONET ST3/SMC), GR-1244-CORE (ST3/ ST4/ST4E)	2	14	6	1 Hz to 650 MHz, Composite Clock (G.703 64 kbps)	1 Hz to 650 MHz, Composite Clock (G.703 64 kbps)	0.23	14	6

To request samples, download documentation, or learn more, visit: **idt.com/go/sync**

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