WM8523

24-bit 192kHz Stereo DAC with 2Vrms Ground Referenced Line Output

DESCRIPTION

The WM8523 is a stereo DAC with integral charge pump and software control interface. This provides 2Vrms line driver outputs using a single 3.3V power supply rail.

The device features ground-referenced outputs and the use of a DC servo to eliminate the need for line driving coupling capacitors and effectively eliminate power on pops and clicks.

The device is controlled and configured either via the I2C/SPI compliant serial control interface or a hardware control interface.

The device supports all common audio sampling rates between 8kHz and 192kHz using all common MCLK fs rates. Master and Slave modes are available and de-emphasis is also supported.

The WM8523 has a 3.3V tolerant digital interface, allowing logic up to 3.3V to be connected.

The device is available in a 20-lead TSSOP package.

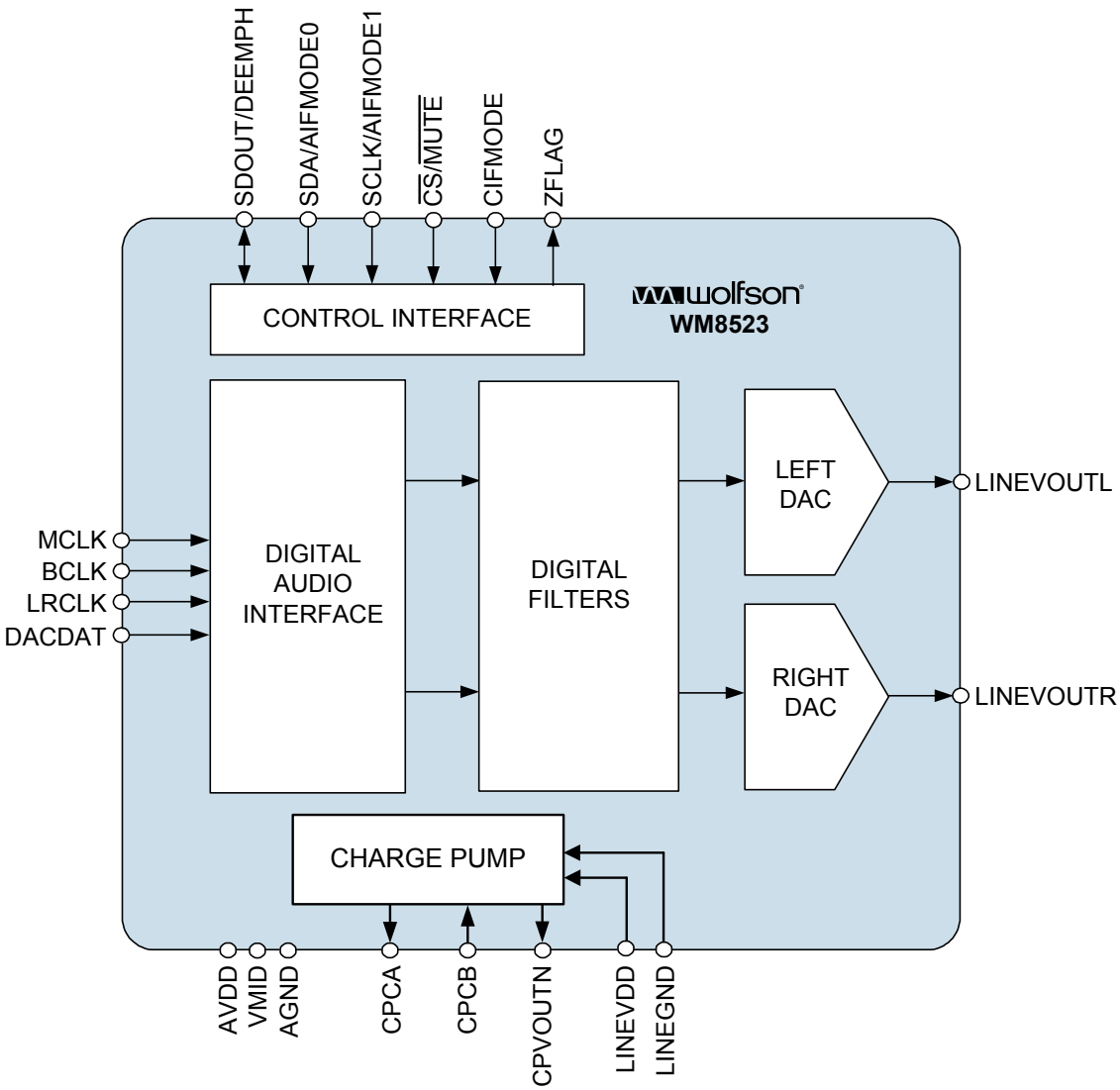
FEATURES

- High performance stereo DAC with ground referenced line driver
- Audio Performance
  - 106dB SNR ('A-weighted')
  - -89dB THD @ -1dBFS
- Digital Volume control ranging from -100dB to +12dB
- 120dB mute attenuation
- All common sample rates from 8kHz to 192kHz supported
- I^2C/SPI compatible and hardware control modes
- Data formats: LJ, RJ, I^2S, DSP
- De-emphasis supported
- Maximum 1mV DC offset on Line Outputs
- Pop/Click suppressed Power Up/Down Sequencer
- AVDD and LINEVDD +3.3V ±10% allowing single supply
- 20-lead TSSOP package
- Operating temperature range: -40°C to 85°C

APPLICATIONS

- Consumer digital audio applications requiring 2Vrms output
  - Set Top Box
  - Digital TV
  - DVD Players
  - Games Consoles
  - A/V Receivers

BLOCK DIAGRAM



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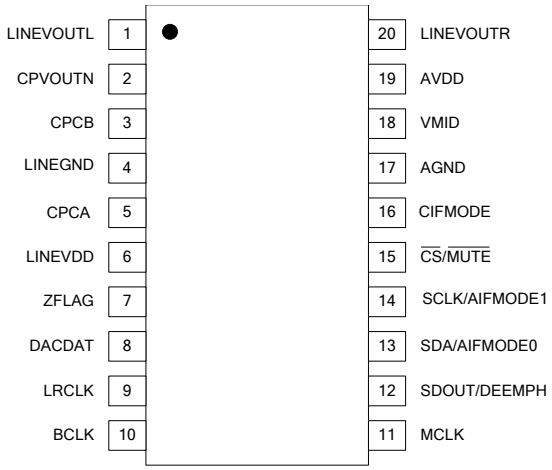
PIN CONFIGURATION



20-LEAD TSSOP

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8523GEDT	−40°C to +85°C	20-lead TSSOP (pb-free)	MSL1	260°C
WM8523GEDT/R	−40°C to +85°C	20-lead TSSOP (pb-free, tape and reel)	MSL1	260°C

Note:

Reel quantity = 2000

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION		
1	LINEVOUTL	Analogue Out	Left line output		
2	CPVOUTN	Analogue Out	Charge Pump negative rail decoupling pin		
3	CPCB	Analogue Out	Charge Pump fly back capacitor pin		
4	LINEGND	Supply	Charge Pump ground		
5	CPCA	Analogue Out	Charge Pump fly back capacitor pin		
6	LINEVDD	Supply	Charge Pump supply		
7	ZFLAG	Digital Out	Zero flag output		
8	DACDAT	Digital In	Digital audio interface data input		
9	LRCLK	Digital I/O	Digital audio interface left/right clock		
10	BCLK	Digital I/O	Digital audio interface bit clock		
11	MCLK	Digital In	Master clock		
			I^2C SOFTWARE MODE	**SPI SOFTWARE MODE**	**HARDWARE MODE**
12	SDOUT/ DEEMPH	Digital I/O	I^2C address select bit[1]	Serial control interface data output pin	0 – No de-emphasis 1 – De-emphasis
13	SDA/ AIFMODE0	Digital I/O Internal pull-down	Serial control interface data input pin	Serial control interface data input pin	**AIFMODE[1:0]** 00 – LJ 24 bits 01 – I2S 24 bits 10 – RJ 16 bits 11 – RJ 24 bits
14	SCLK/ AIFMODE1	Digital I/O Internal pull-down	Serial control interface clock input pin	Serial control interface clock input pin	
15	$\overline{CS}$/ $\overline{MUTE}$	Digital In	I^2C address select bit[0]	Serial control interface chip select	0 – Mute enabled 1 – Mute disabled
16	CIFMODE	Digital In Tri-level	0 – I^2C compatible mode select	1 – SPI compatible mode select	Z – Hardware mode
17	AGND	Supply	Analogue ground		
18	VMID	Analogue Out	Analogue midrail decoupling pin		
19	AVDD	Supply	Analogue supply		
20	LINEVOUTR	Analogue Out	Right line output		

Note: Tri-level pins which require the 'Z' state to be selected should be left floating (open)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
AVDD, LINEVDD	-0.3V	+4.5V
Voltage range digital inputs	LINEGND -0.3V	LINEVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Temperature range, T_A	-40°C	+125°C
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue grounds must always be within 0.3V of each other.
2. LINEVDD and AVDD must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue supply range	AVDD, LINEVDD		2.97	3.3	3.63	V
Ground	AGND, LINEGND			0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

LINEVDD=AVDD=3.3V, LINEGND=AGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Output Levels						
Output Level		0dBFS	1.89	2.1	2.31	Vrms
Load Impedance			1			kΩ
Load Capacitance		No external RC filter			300	pF
		With filter shown in Figure 39.			1	µF
DAC Performance						
Signal to Noise Ratio	SNR	R_L = 10kΩ A-weighted	100	106		dB
		R_L = 10kΩ Un-weighted		104		dB
Dynamic Range	DNR	R_L = 10kΩ A-weighted		104		dB
Total Harmonic Distortion	THD	R_L = 10kΩ -1dBFS		-89		dB
		R_L = 10kΩ 0dBFS		-86		dB
AVDD + LINEVDD Power Supply Rejection Ratio	PSRR	100Hz		54		dB
		1kHz		54		dB
		20kHz		50		dB
Channel Separation		1kHz		100		dB
		20Hz to 20kHz		95		dB
System Absolute Phase				0		degrees
Channel Level Matching				0.1		dB
Mute Attenuation				-120		dB
DC Offset at LINEVOUTL and LINEVOUTR			-1	0	1	mV
Digital Logic Levels						
Input HIGH Level	V_{IH}		0.7× LINEVDD			V
Input LOW Level	V_{IL}				0.3× LINEVDD	V
Output HIGH Level	V_{OH}	I_{OL} = 1mA	0.9× LINEVDD			V
Output LOW Level	V_{OL}	I_{OH} = -1mA			0.1× LINEVDD	V
Input Capacitance				10		pF
Input Leakage			-0.9		0.9	µA

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum theoretical full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
4. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.

POWER CONSUMPTION MEASUREMENTS

Test Conditions LINEVDD=AVDD=3.3V, LINEGND=AGND=0V, T_A=+25°C, Slave Mode, quiescent (no signal)				
	TEST CONDITIONS	**IAVDD (mA)**	**ILINEVDD (mA)**	**TOTAL (mA)**
Off	No clocks applied SYS_ENA[1:0]=00	0.8	1.1	1.9
fs=48kHz, MCLK=256fs				
Standby	SYS_ENA[1:0]=01	0.2	2.2	2.4
Playback	SYS_ENA[1:0]=11	4.8	6.0	10.8
fs=96kHz, MCLK=256fs				
Standby	SYS_ENA[1:0]=01	0.2	2.9	3.1
Playback	SYS_ENA[1:0]=11	5.5	8.5	14.0
fs=192kHz, MCLK=128fs				
Standby	SYS_ENA[1:0]=01	0.2	2.9	3.1
Playback	SYS_ENA[1:0]=11	5.5	8.5	14.0

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

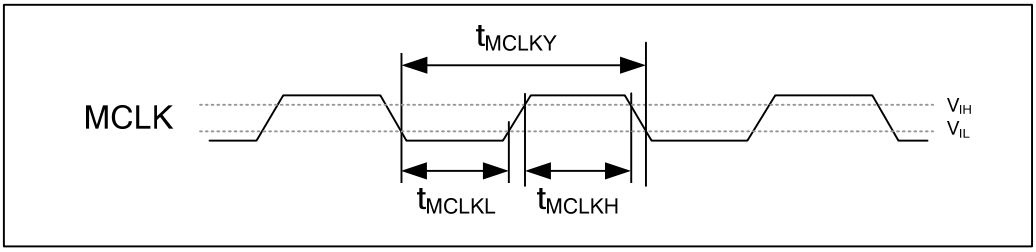


Figure 1 System Clock Timing Requirements

Test Conditions

LINEVDD=AVDD=2.97~3.63V, LINEGND=AGND=0V, T_A=+25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Master Clock Timing Information					
MCLK cycle time	t_{MCLKY}	27		500	ns
MCLK high time	t_{MCLKH}	11			ns
MCLK low time	t_{MCLKL}	11			ns
MCLK duty cycle (t_{MCLKH}/t_{MCLKL})		40:60		60:40	%

AUDIO INTERFACE TIMING – MASTER MODE

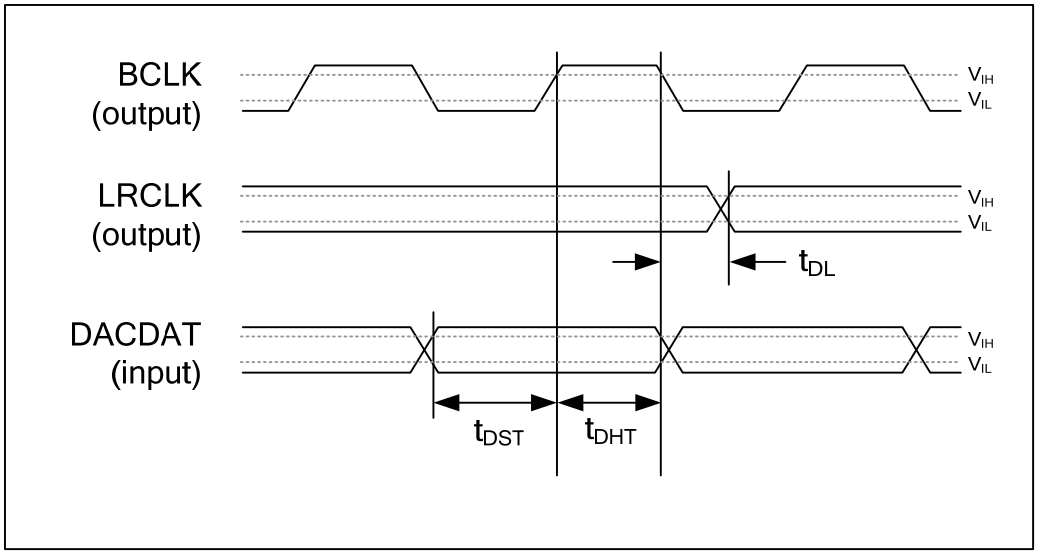


Figure 2 Master Mode Digital Audio Data Timing

Test Conditions

LINEVDD=AVDD=2.97~3.63, LINEGND=AGND=0V, T_A=+25°C, Master Mode

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
LRCLK propagation delay from BCLK falling edge	t_{DL}	4		16	ns
DACDAT setup time to BCLK rising edge	t_{DST}	22			ns
DACDAT hold time to BCLK falling edge	t_{DHT}	25			ns

Table 1 Master Mode Audio Interface Timing

AUDIO INTERFACE TIMING – SLAVE MODE

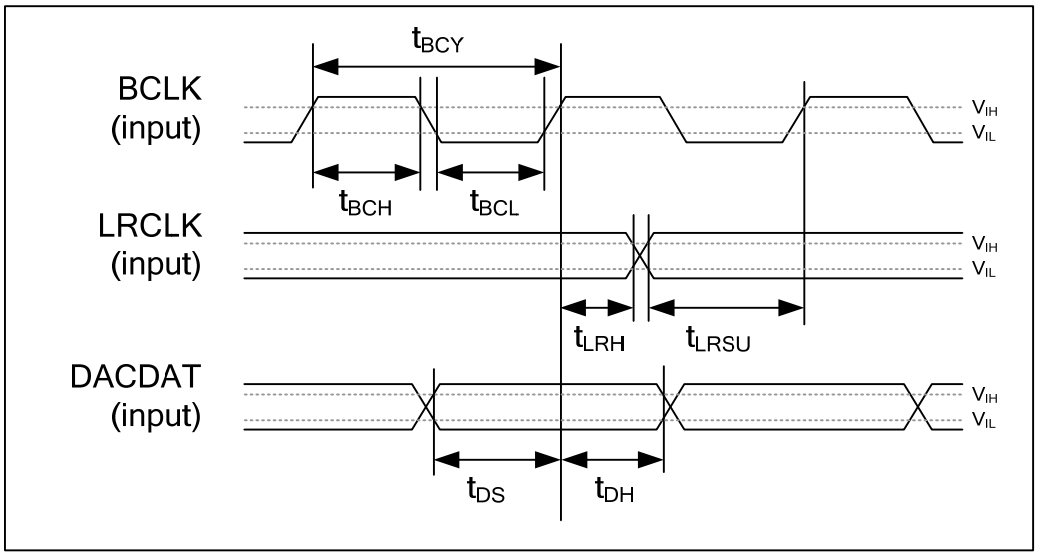


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

LINEVDD=AVDD=2.97~3.63V, LINEGND=AGND=0V, T_A=+25°C, Slave Mode

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	27			ns
BCLK pulse width high	t_{BCH}	11			ns
BCLK pulse width low	t_{BCL}	11			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	7			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	5			ns
DACDAT hold time from LRCLK rising edge	t_{DH}	5			ns
DACDAT set-up time to BCLK rising edge	t_{DS}	7			ns

Table 2 Slave Mode Audio Interface Timing

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – I²C MODE

I²C mode is selected by driving the CIFMODE pin low.

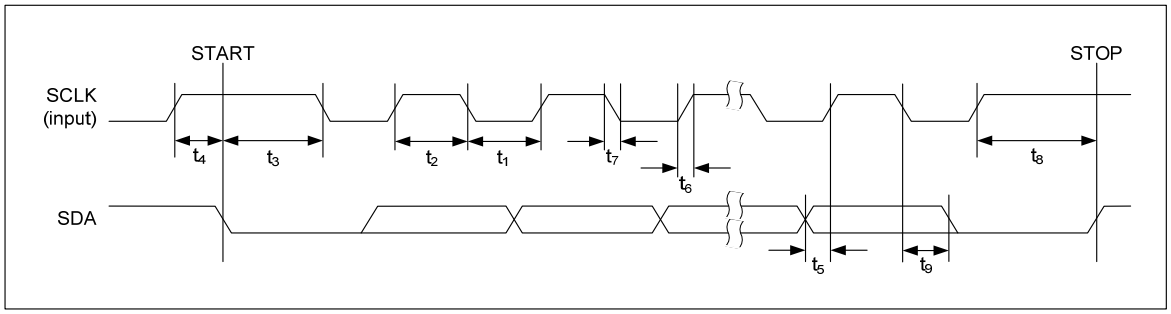


Figure 4 Control Interface Timing – I²C Control Mode

Test Conditions

LINEVDD=AVDD=2.97~3.63V, LINEGND=AGND=0V, T_A=+25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency				400	kHz
SCLK Low Pulse-Width	t_1	100			ns
SCLK High Pulse-Width	t_2	100			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDA, SCLK Rise Time	t_6			300	ns
SDA, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed		2		8	ns

Table 3 Control Interface Timing – I²C Control Mode

CONTROL INTERFACE TIMING – SPI MODE

SPI mode is selected by connecting the CIFMODE pin high.

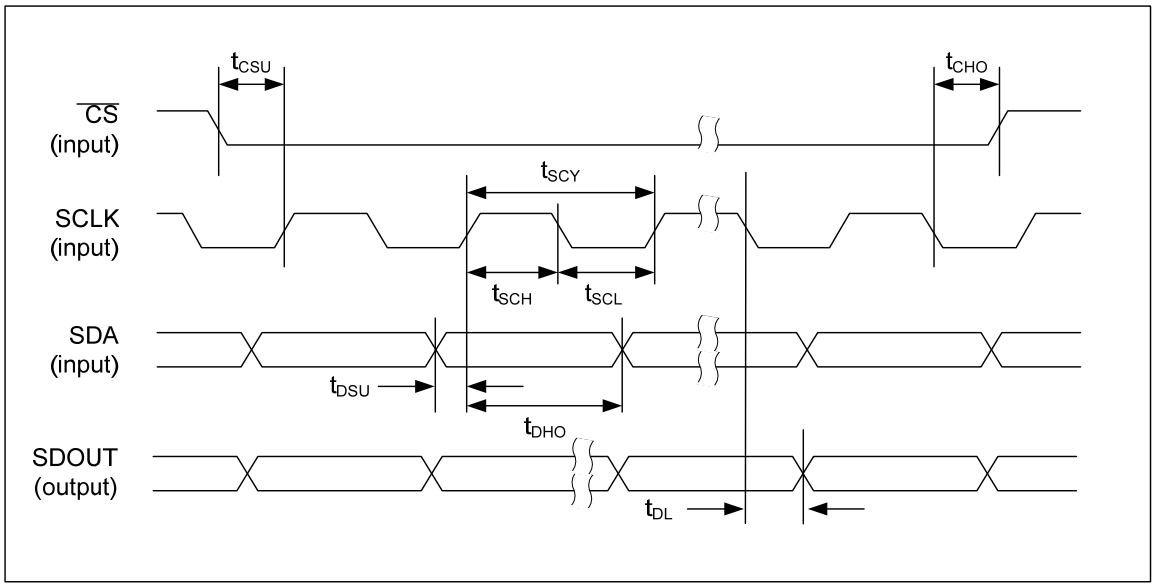


Figure 5 Control Interface Timing – SPI Control Mode (Read Cycle)

Test Conditions

LINEVDD=AVDD=2.97~3.63V, LINEGND=AGND=0V, T_A=+25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB falling edge	t_{CSU}	40			ns
SCLK falling edge to CSB rising edge	t_{CHO}	40			ns
SCLK pulse cycle time	t_{SCY}	160			ns
SCLK pulse width low	t_{SCL}	64			ns
SCLK pulse width high	t_{SCH}	64			ns
SDA to SCLK set-up time	t_{DSU}	20			ns
SDA to SCLK hold time	t_{DHO}	40			ns
SDOUT propagation delay from SCLK falling edge	t_{DL}			5	ns
Pulse width of spikes that will be suppressed	t_{ps}	2		8	ns

Table 4 Control Interface Timing –SPI Control Mode

POWER ON RESET CIRCUIT

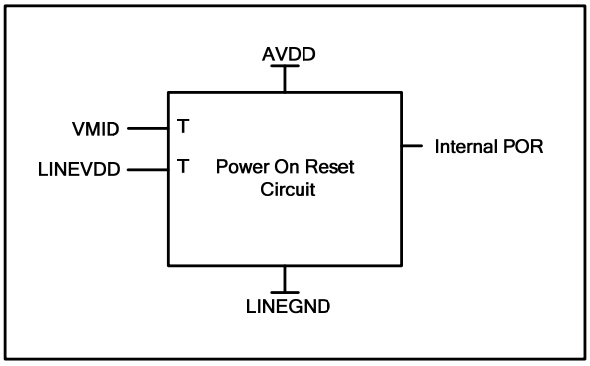


Figure 6 Internal Power on Reset Circuit Schematic

The WM8523 includes an internal Power-On-Reset circuit, as shown in Figure 6, which is used to reset the DAC digital logic into a default state after power up. The POR circuit is powered by AVDD and has as its inputs VMID and LINEVDD. It asserts POR low if VMID or LINEVDD are below a minimum threshold.

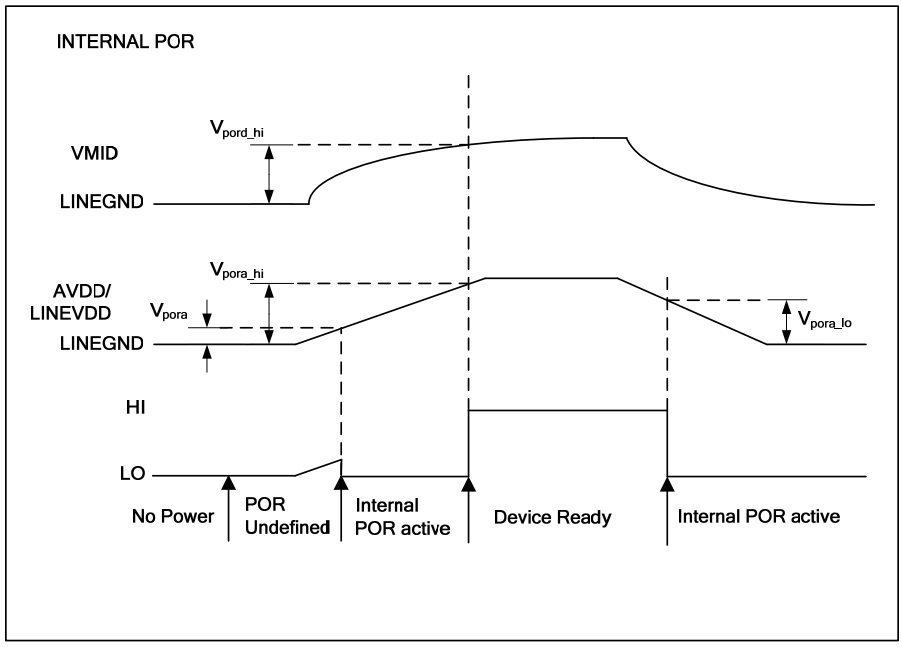


Figure 7 Typical Power Timing Requirements

Figure 7 shows a typical power-up sequence where LINEVDD comes up with AVDD. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee POR is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. After VMID rises to V_{pord_hi} and AVDD rises to $V_{pora\_hi,}$ POR is released high and all registers are in their default state and writes to the control interface may take place.

On power down, PORB is asserted low whenever LINEVDD or AVDD drop below the minimum threshold V_{pora_low}.

Test Conditions

LINEVDD = AVDD = 3.3V AGND = LINEGND = 0V, T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
VDD level to POR defined (LINEVDD/AVDD rising)	V_{pora}	Measured from LINEGND		158		mV
VDD level to POR rising edge (VMID rising)	V_{pord_hi}	Measured from LINEGND	0.63	0.8	1	V
VDD level to POR rising edge (LINEVDD/AVDD rising)	V_{pora_hi}	Measured from LINEGND	1.44	1.8	2.18	V
VDD level to POR falling edge (LINEVDD/AVDD falling)	V_{pora_lo}	Measured from LINEGND	0.96	1.46	1.97	V

Table 5 Power on Reset

Note: All values are simulated results

DEVICE DESCRIPTION

INTRODUCTION

The WM8523 provides high fidelity, $2V_{rms}$ ground referenced stereo line output from a single supply line with minimal external components. The integrated DC servo eliminates the requirement for external mute circuitry by minimising DC transients at the output during power up/down. The device is well-suited to both stereo and multi-channel systems.

The device supports all common audio sampling rates between 8kHz and 192kHz using common MCLK fs rates. Master and slave modes are available.

The WM8523 supports both hardware and software control modes.

In hardware control mode, the digital audio interface format is switchable between 16 to 24bits LJ, RJ and I^2S. Mute and de-emphasis control pins are also available.

In software control modes the digital audio interface is highly programmable, with four control interface addresses to allow multiple WM8523 devices to be configured independently.

SOFTWARE CONTROL INTERFACE

Software Control Mode is selected by logic 1 or 0 on the CIFMODE pin. The logic level is referenced to the LINEVDD power domain. When software mode is selected, the associated multi-function control pins are defined as described in Table 6.

PIN NAME	PIN NUMBER	DESCRIPTION
SDOUT	12	I^2C Mode - Device Address[1] SPI Mode - Serial Data Output
SDA	13	Serial Data Input
SCLK	14	Serial Data Clock
$\overline{CS}$	15	I^2C Mode - Device Address[0] SPI Mode - Chip Select
CIFMODE	16	Control Interface Mode 0 = I^2C Mode 1 = SPI Mode Z = Hardware Mode

Table 6 Software Control Pin Configuration

In software control mode, the WM8523 is controlled by writing to its control registers. Readback is available for all registers, including device ID and power management status bits. The control interface can operate as an I^2C or SPI control interface: register read-back is provided on the bi-directional pin SDA in I^2C mode, and on the SDOUT pin in SPI mode. The WM8523 software control interface is supplied by the LINEVDD power domain.

The available software control interface modes are summarised as follows:

- I^2C mode uses pins SCLK and SDA.
- SPI mode uses pins $\overline{CS}$, SCLK and SDA and SDOUT.

I^2C mode is selected by setting the CIFMODE pin to logic 0. When CIFMODE is set to logic 1, SPI mode is selected.

I²C CONTROL MODE

In I²C mode, the WM8523 is a slave device on the control interface; SCLK is a clock input, while SDA is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM8523 transmits logic 1 by tri-stating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the logic 1 can be recognised by the master.

In order to allow many devices to share a single I²C control bus, every device on the bus has a unique 7-bit device address (this is not the same as the 8-bit address of each register in the WM8523). The device address is determined by the logic level on the SDOUT and $\overline{CS}$ pins as shown in Table 7. The LSB of the device address is the R/$\overline{W}$ bit; this bit is set to logic 1 for "Read" and logic 0 for "Write".

SDOUT ADDR1	$\overline{CS}$ ADDR0	DEVICE ADDRESS
0	0	0011 0100 (34h)
0	1	0011 0110 (36h)
1	0	0011 1100 (3Ch)
1	1	0011 1110 (3Eh)

Table 7 Control Interface Device Address Selection

The WM8523 operates as an I²C slave device only. The controller indicates the start of data transfer with a high to low transition on SDA while SCLK remains high. This indicates that a device address, register address and data will follow. All devices on the I²C bus respond to the start condition and shift in the next eight bits on SDA (7-bit device address + Read/Write bit, MSB first). If the device address received matches the device address of the WM8523, then the WM8523 responds by pulling SDA low on the next clock pulse (ACK). If the device address is not recognised or the R/$\overline{W}$ bit is '1' when operating in write only mode, the WM8523 returns to the idle condition and waits for a new start condition and valid address.

If the device address matches the device address of the WM8523, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDA while SCLK remains high. After receiving a complete address and data sequence the WM8523 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDA changes while SCLK is high), the device returns to the idle condition.

The WM8523 supports the following read and write operations:

- Single write
- Single read

The sequence of signals associated with a single register write operation is illustrated in Figure 8.

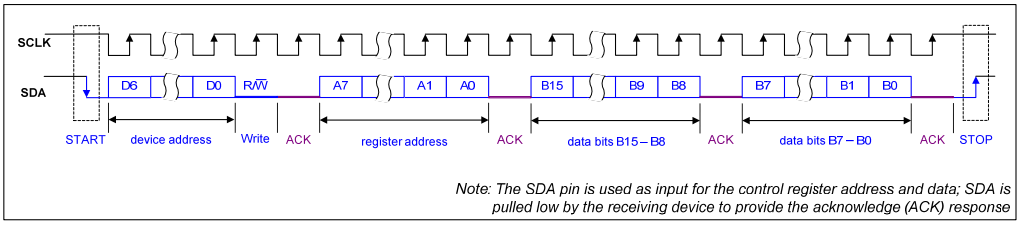


Figure 8 Control Interface I²C Register Write

The sequence of signals associated with a single register read operation is illustrated in Figure 9.

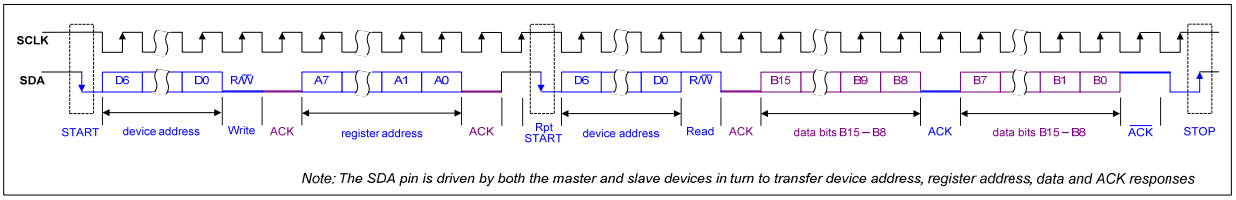


Figure 9 Control Interface I²C Register Read

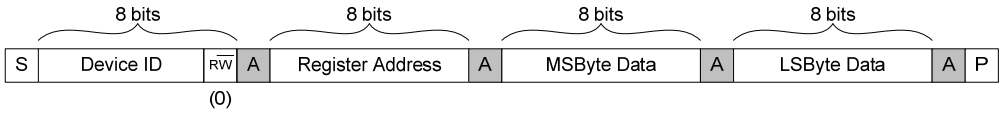


Figure 10 Single Register Write to Specified Address

Figure 11 Single Register Read from Specified Address

SPI CONTROL MODE

The WM8523 can also be controlled by writing to registers through a SPI control interface. A control word consists of 24 bits. The first bit is the read/write bit (R/$\overline{W}$), which is followed by 7 address bits (A6 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

Volume update registers R06h and R07h are unavailable in SPI control mode. To use volume update in software control mode, I^2C mode must be used.

In SPI mode, every rising edge of SCLK clocks in one data bit from the SDA pin. A rising edge on $\overline{CS}$ latches in a complete control word consisting of the last 24 bits.

The SPI mode write operation protocol is illustrated in Figure 12.

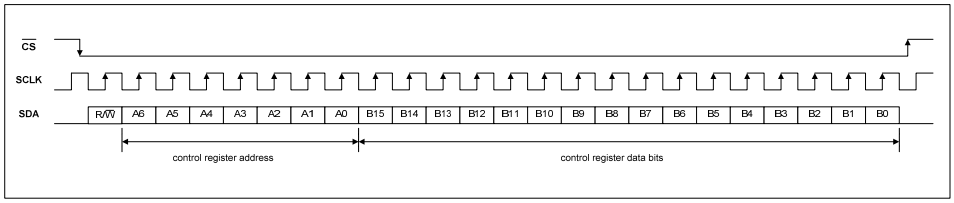


Figure 12 SPI Control Interface – write operation

In Write operations (R/$\overline{W}$=0), all SDA bits are driven by the controlling device.

In Read operations (R/$\overline{W}$=1), the SDA pin is ignored following receipt of the valid register address. The data bits are output by the WM8523 on the SDOUT pin.

The SPI mode read operation protocol is illustrated in Figure 13.

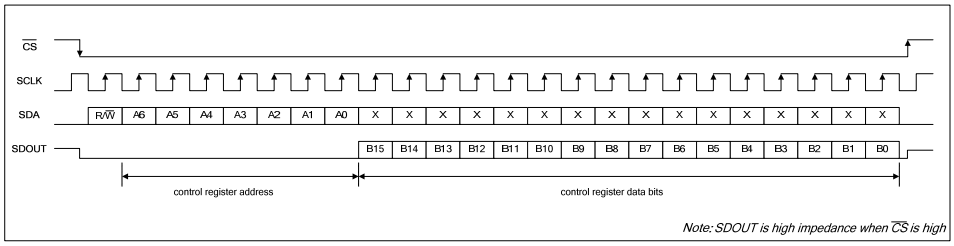


Figure 13 SPI Control Interface – read operation

REGISTER RESET

Any write to register R0 (00h) will reset the WM8523. All register bits are reset to their default values.

DEVICE ID AND REVISION

Reading from register R0 (00h) returns the device ID. Reading from register R1 returns the device revision number.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 DEVICE_ID 00h	15:0	DEVICE_ID [15:0]	10000101 00100011	**Device ID** A read of this register will return the device ID, 0x8523.
R1 REVISION 01h	2:0	CHIP_REV [2:0]	N/A	**Device Revision** A read of this register will return the device revision number. This number is sequentially incremented if the device design is updated.

Table 8 Device ID and Revision Number

DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting audio data to the WM8523. The digital audio interface uses three pins:

- DACDAT: DAC data input
- LRCLK: Left/Right data alignment clock
- BCLK: Bit clock, for synchronisation

In software control mode, all interface data formats and modes of operation can be selected. In hardware control mode, only a subset of formats and modes are supported – see the Hardware Interface Control section on page 30 for details.

MASTER AND SLAVE MODE OPERATION

The WM8523 digital audio interface can operate as a master or as a slave as shown in Figure 14 and Figure 15.

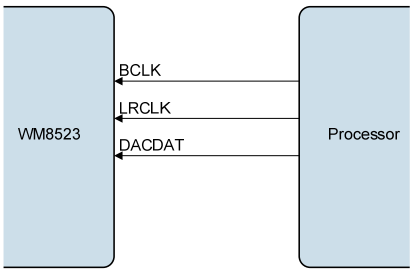


Figure 14 Slave Mode

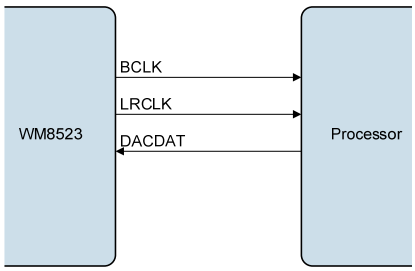


Figure 15 Master Mode

INTERFACE FORMATS

The WM8523 supports five different audio data formats:

- Left justified
- Right justified
- I^2S
- DSP Mode A
- DSP Mode B

PCM operation is supported using the DSP mode. All seven of these modes are MSB first. They are described in Audio Data Formats on page 20. Refer to the "Electrical Characteristics" section for timing information. Refer to Table 10 for interface control format register settings.

AUDIO DATA FORMATS

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.

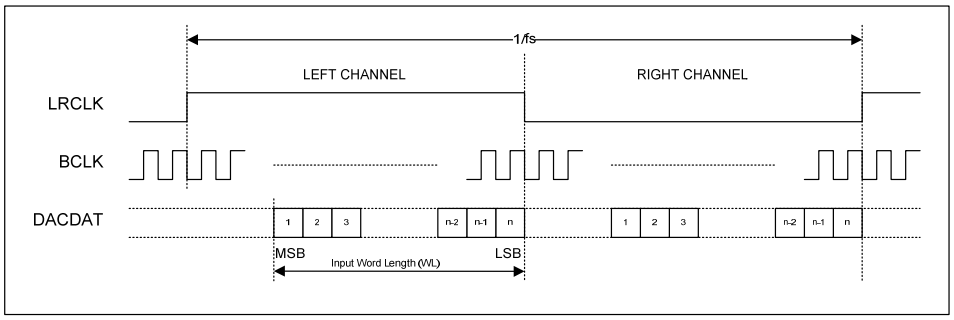


Figure 16 Right Justified Audio Interface (assuming n-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

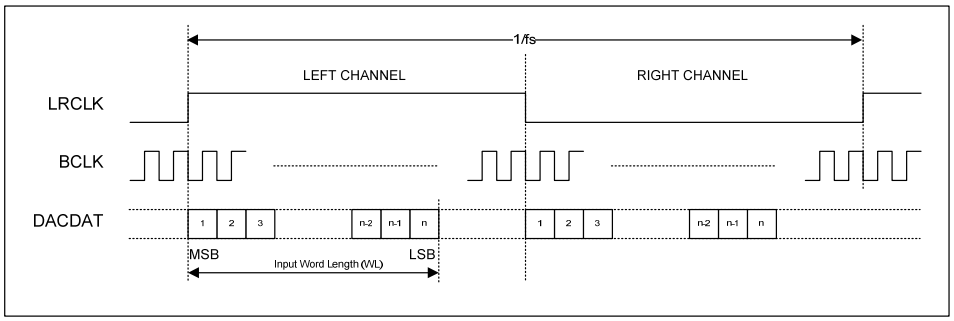


Figure 17 Left Justified Audio Interface (assuming n-bit word length)

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

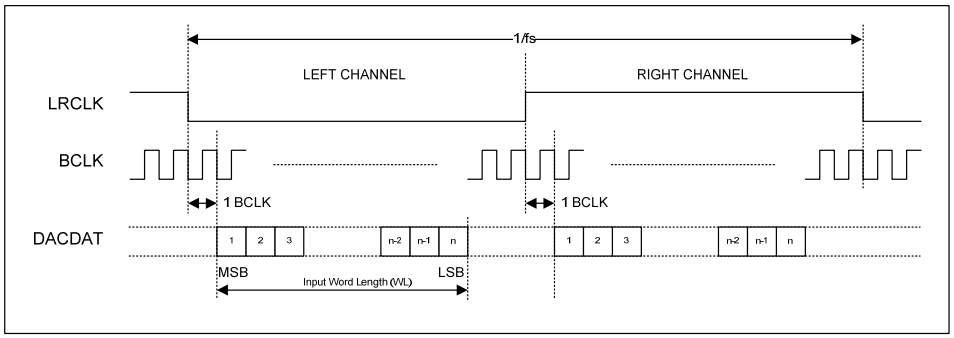


Figure 18 I^2S Justified Audio Interface (assuming n-bit word length)

In DSP mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by AIF_LRCLK_INV) following a rising edge of LRCLK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRCLK output will resemble the frame pulse shown in Figure 19 and Figure 20. In device slave mode, Figure 21 and Figure 22, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

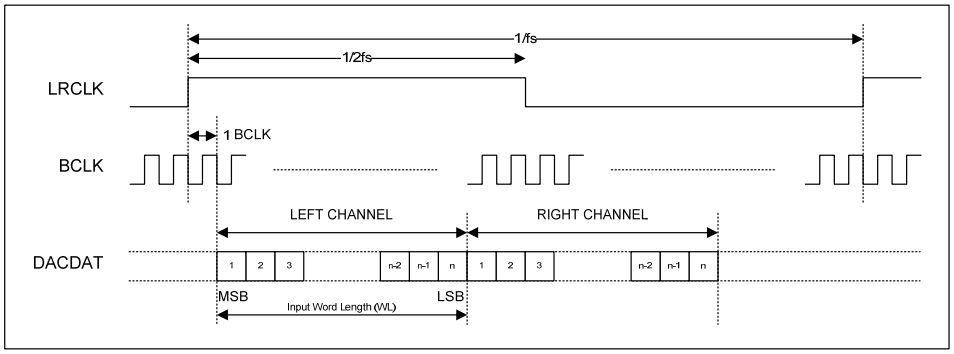


Figure 19 DSP Mode Audio Interface (mode A, AIF_LRCLK_INV=0, Master)

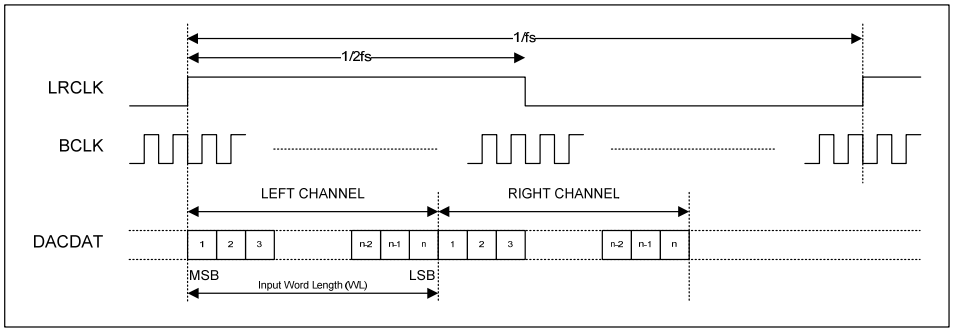


Figure 20 DSP Mode Audio Interface (mode B, AIF_LRCLK_INV=1, Master)

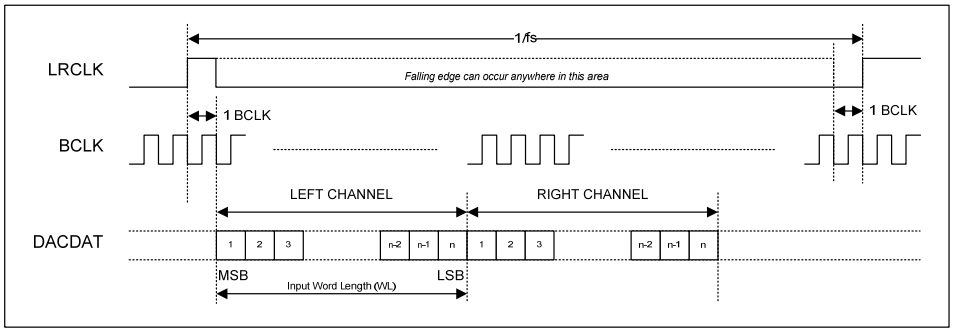


Figure 21 DSP Mode Audio Interface (mode A, AIF_LRCLK_INV=0, Slave)

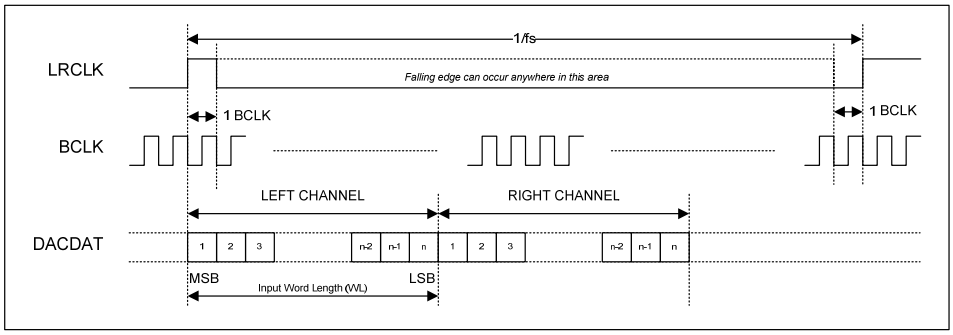


Figure 22 DSP Mode Audio Interface (mode B, AIF_LRCLK_INV=1, Slave)

DIGITAL AUDIO INTERFACE CONTROL

The control of the audio interface in software mode is achieved by register write. Dynamically changing the audio data format may cause erroneous operation and is not recommended.

Digital audio data is transferred to the WM8523 via the digital audio interface. The DAC operates in master or slave mode.

The DAC audio interface requires left/right frame clock (LRCLK) and bit clock (BCLK). These can be supplied externally (slave mode) or they can be generated internally (master mode). Selection of master and slave mode is achieved by setting AIF_MSTR bit in Register 3.

The frequency of LRCLK in master mode is dependent upon the DAC master clock frequency and the AIF_SR[2:0] bits. The frequency of BCLK in master mode can be selected by AIF_BCLKDIV[2:0]. In slave mode, the MCLK to LRCLK ratio can be auto-detected or set manually using the AIF_SR[2:0] bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 AIF_CTRL1 03h	7	AIF_MSTR	0	**Master/Slave Select** 0 = Slave 1 = Master
R4 AIF_CTRL2 04h	2:0	AIF_SR[2:0	000	**MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs
	5:3	AIF_BCLKDIV[2:0]	000	**BCLK Divider Control (Master Mode)** 000 = MCLK/4 001 = MCLK/8 010 = 32fs 011 = 64fs 100 = 128fs 101 - 111 reserved

Table 9 DAC Clocking Mode Control

Interface timing is such that the input data and left/right clock are sampled on the rising edge of BCLK. By setting the appropriate BCLK and LRCLK polarity bits, the WM8523 DAC can sample data on the opposite clock edges.

The control of audio interface formats and clock polarities is summarised in Table 10.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 AIF_CTRL1 03h	1:0	AIF_FMT	10	**Audio Data Interface Format** 00 = Right justified 01 = Left justified 10 = I2S format 11 = DSP mode
	2	Reserved	0	Reserved
	4:3	AIF_WL	10	**Audio Data Word Length** 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits
	5	AIF_BCLK_INV	0	**BCLK Inversion Control** Slave mode: 0 = use rising edge 1 = use falling edge Master mode: 0 = BCLK normal 1 = BCLK inverted
	6	AIF_LRCLK_INV	0	**LRCLK Inversion Control** 0 = normal polarity 1 = inverted polarity When AIF_FMT[2:0]=011 (DSP Mode): 0 = mode A (2nd clock) 1 = mode B (1st clock)

Table 10 Audio Interface Control

DIGITAL AUDIO DATA SAMPLING RATES

The external master clock is applied directly to the MCLK input pin. In a system where there are a number of possible sources for the reference clock, it is recommended that the clock source with the lowest jitter be used for the master clock to optimise the performance of the WM8523.

In slave mode the WM8523 has a detection circuit that automatically determines the relationship between the master clock frequency (MCLK) and the sampling rate (LRCLK), to within ±32 system clock periods. The MCLK must be synchronised with the LRCLK, although the device is tolerant of phase variations or jitter on the MCLK.

If the device is configured in slave mode using auto-detect or in hardware mode, and during sample rate change the ratio between MCLK and LRCLK varies more than once within 1026 LRCLK periods, then it is recommended that the device be taken into the standby state or the off state before the sample rate change and held in standby until the sample rate change is complete. This will ensure correct operation of the detection circuit on the return to the enabled state. For details on the standby state, please refer to the Software Control Interface (software mode, page 15) and Power Up and Down Control In Hardware Mode section of the datasheet (hardware mode, on page 31).

The DAC supports MCLK to LRCLK ratios of 128fs to 1152fs and sampling rates of 8kHz to 192kHz, provided the internal signal processing of the DAC is programmed to operate at the correct rate.

Table 11 shows typical master clock frequencies and sampling rates supported by the WM8523 DAC.

SAMPLING RATE LRCLK	MASTER CLOCK FREQUENCY (MHz)						
	128fs	192fs	256fs	384fs	512fs	768fs	1152fs
8kHz	Unavailable	Unavailable	2.048	3.072	4.096	6.144	9.216
32kHz	Unavailable	Unavailable	8.192	12.288	16.384	24.576	36.864
44.1kHz	Unavailable	Unavailable	11.2896	16.9344	22.5792	33.8688	Unavailable
48kHz	Unavailable	Unavailable	12.288	18.432	24.576	36.864	Unavailable
88.2kHz	11.2896	16.9344	22.5792	33.8688	Unavailable	Unavailable	Unavailable
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable	Unavailable
176.4kHz	22.5792	33.8688	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable

Table 11 MCLK Frequencies and Audio Sample Rates

DAC FEATURES

SYSTEM ENABLE

The WM8523 includes a number of enable and disable mechanisms to allow the device to be powered on and off in a pop-free manner. The SYS_ENA[1:0] control bits enable the DAC and analogue paths.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 PSCTRL1 02h	1:0	SYS_ ENA[1:0]	00	**System Power Control** 00 = Off 01 = Power down 10 = Power up and mute 11 = Power up and unmute

Table 12 System Enable Control

Note: MCLK must be present at all times when using the SYS_ENA[1:0] bits. If MCLK is stopped at any point the device will power down to the 'off' state, but all register settings will remain. Restarting MCLK will start the device internal power sequence and the device will return to the power state set by the SYS_ENA[1:0] bits.

The power up and power down sequences are summarised in Figure 23. There is no requirement to manually cycle the device through the sequence via register writes, as the device will always automatically step through each stage in the sequence.

Power Up

When SYS_ENA[1:0]=00, the internal clocks are stopped and all analogue and digital blocks are disabled for maximum power saving. The device starts up in this state in software mode. Setting SYS_ENA[1:0]=01 enables the internal charge pump and required control circuitry, but the signal path remains powered down. When SYS_ENA[1:0]=10 all blocks are powered up sequentially and full system configuration is achieved. Once this is complete, the device is ready to pass audio but is muted. Setting SYS_ENA[1:0]=11 releases the mute and audio playback begins.

Power Down

When SYS_ENA[1:0]=11 the device is powered up and passing audio. Changing SYS_ENA[1:0]=10 applies a digital softmute to the output. Setting SYS_ENA[1:0]=01 sequentially powers down all circuit blocks but leaves the charge pump and required control circuitry enabled. This can be considered the low-power standby state. Finally, setting SYS_ENA[1:0]=00 will disable all circuit blocks including the charge pump, and full system initialisation will be required to restart the device.

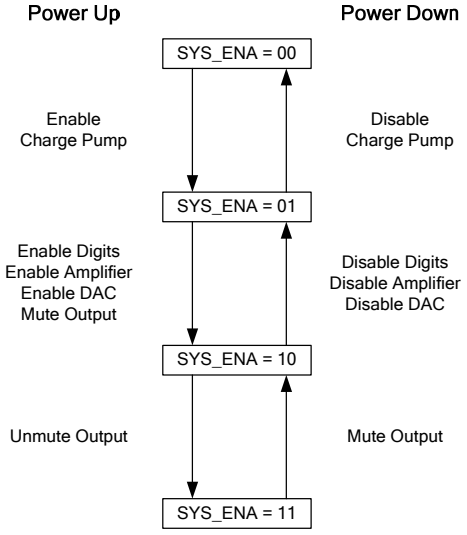


Figure 23 SYS_ENA[1:0] Power Up and Down Sequences

DIGITAL VOLUME CONTROL

The WM8523 DAC includes digital volume control, allowing the digital gain to be adjusted between −100dB and +12dB in 0.25dB steps. Volume update bits allow the user to write both left and right channel volume changes before the volume is updated. Digital volume control is only available in I^2C mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 DAC_GAINL 06h	8:0	DACL _VOL[8:0]	110001000	**DAC Digital Volume** 0 0000 0000 = −100dB 0 0000 0001 = −99.75dB 0 0000 0010 = −99.5dB …0.25dB steps 1 1001 0000 = 0dB …0.25dB steps 1 1011 1110 = +11.75dB 1 11XX XXXX = +12dB
R7 DAC_GAINR 07h	8:0	DACR _VOL[8:0]		
R6 DAC_GAINL 06h	9	DACL_VU	0	**DAC Digital Volume Update** 0 = Latch DAC volume setting into Register Map but do not update volume 1 = Latch DAC volume setting into Register Map and update left and right channels simultaneously
R7 DAC_GAINR 07h	9	DACR_VU	0	

Table 13 DAC Digital Volume Control

VOLUME CHANGE MODES

Volume can be adjusted by step change (either using zero cross or not) or by soft ramp. The volume change mode is controlled by the DAC_VOL_DOWN_RAMP and DAC_VOL_UP_RAMP bits in R5:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 DAC_CTRL3 05h	0	DAC_VOL _DOWN_ RAMP	1	**DAC Digital Volume Decrease Control** 0 = apply volume decreases instantly (step) 1 = ramp volume decreases
	1	DAC_VOL _UP_ RAMP	0	**DAC Digital Volume Increase Control** 0 = apply volume increases instantly (step) 1 = ramp volume increases

Table 14 Volume Ramp Control

Figure 24 illustrates the effect of the volume ramp:

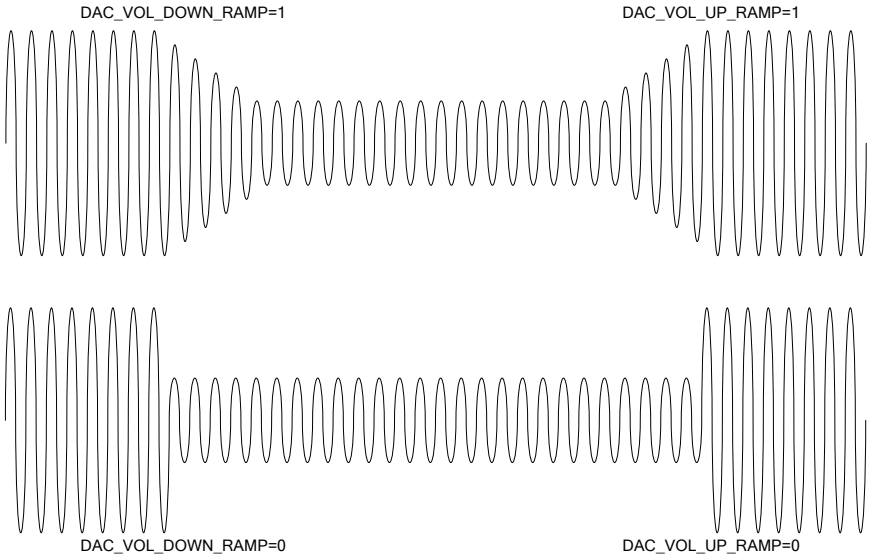


Figure 24 Volume Ramp Functionality

Ramp Volume Changes

If ramp volume changes are selected, the ramp rate is dependent upon the sampling rate. The ramp rates for common audio sample rates are shown in Table 15.

SAMPLE RATE FOR DAC (kHz)	GAIN RAMP RATE (ms/dB)
8	1
32	0.25
44.1	0.18
48	0.17
88.2	0.1
96	0.08
176.4	0.05
192	0.04

Table 15 Volume Ramp Rate

For example, when using a sample rate of 48kHz, the time taken for a volume change from an initial setting of 0dB to -20dB is calculated as follows:

Volume Change (dB) x Volume Ramp Rate (ms/dB) = 20 x 0.17 = 3.4ms

Zero cross is not used when ramping. The volume level in the DAC is set by the user in 0.25dB increments, but during the volume ramp increments of 0.125dB are actually used. This step size is inaudible and means there is no requirement to wait until a zero crossing occurs. Another benefit of not using zero cross when ramping is that predictable ramp times are produced – there is no signal dependency on the ramp time.

Step Volume Changes and Zero Cross

The step volume control includes optional zero cross functionality. When zero cross is enabled, by setting DAC_ZCEN=1, volume changes are not applied until the signal crosses zero so no discontinuity is seen in the output signal. Zero cross helps to prevent pop and click noise when changing volume settings and is therefore recommended if using step volume changes.

The zero cross function includes a timeout which forces volume changes if a zero cross event does not occur. The timeout period is 14400 samples, equivalent to 300ms at 48kHz sample rate.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 DAC_CTRL3 05h	4	DAC_ ZCEN	0	**Zero Cross Enable** 0 = Do not use zero cross 1 = Use zero cross

Table 16 Zero Cross Control

Table 17 gives a summary of the volume mode settings and their effect.

DAC_VOL_ UP_RAMP	DAC_VOL_ DOWN_RAMP	DAC_ZCEN	VOLUME CHANGE UP	VOLUME CHANGE DOWN
0	0	0	Step, no zero cross	Step, no zero cross
0	1	0	Step, no zero cross	Ramp
1	0	0	Ramp	Step, no zero cross
1	1	0	Ramp	Ramp
0	0	1	Step, use zero cross	Step, use zero cross
0	1	1	Step, use zero cross	Ramp
1	0	1	Ramp	Step, use zero cross
1	1	1	Ramp	Ramp

Table 17 Volume Change Summary

MUTE

A digital mute can be applied to left and right channels independently.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 DAC_CTRL3 05h	2	DACL_ MUTE	0	**Left DAC Mute** 0 = Normal operation 1 = Mute
R5 DAC_CTRL3 05h	3	DACR_ MUTE	0	**Right DAC Mute** 0 = Normal operation 1 = Mute

Table 18 DAC Mute Control

The DAC mute function in software mode is controlled by the register settings DAC_VOL_UP_RAMP, DAC_VOL_DOWN_RAMP and DAC_ZCEN as described in Table 17**.**

DIGITAL MONOMIX CONTROL

The DAC can be set to output a range of mono and stereo options using DAC_OP_MUX[1:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 AIF_CTRL2 04h	7:6	DAC_OP_ MUX[1:0]	00	**DAC Digital Monomix** 00 = Stereo (Normal Operation) 01 = Mono (Left data to DACR) 10 = Mono (Right data to DACL) 11 = Digital Monomix, (L+R)/2

Table 19 Digital Monomix Control

DE-EMPHASIS

A digital de-emphasis filter may be applied to the DAC output when the sampling frequency is 44.1kHz. Operation at 48kHz and 32kHz is also possible, but with an increase in the error from the ideal response. Details of the de-emphasis filter characteristic for 32kHz, 44.1kHz and 48kHz can be seen in Figure 31 to Figure 36.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 AIF_CTRL1 03h	6	DAC _DEEMP	0	**DAC De-emphasis** 0 = No de-emphasis 1 = Apply de-emphasis

Table 20 De-emphasis Control

ZERO DETECT

The infinite zero detect allows the user to select the number of zero samples received before the ZFLAG pin is asserted high, as described in Table 21.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 ZERO_DETECT 08h	0	ZD_ COUNT	0	**Zero Detect Count Control** 0 = 1024 1 = 2048

Table 21 Zero Detect Control

HARDWARE CONTROL INTERFACE

The WM8523 can be controlled in hardware mode or in software modes. In hardware mode, the device is configured according to logic levels applied to hardware pins.

Hardware control mode is selected by leaving CIFMODE pin open-circuit (high-impedance). When hardware mode is selected, the associated multi-function control pins are defined as described in Table 22.

PIN NAME	PIN NUMBER		DESCRIPTION		
PIN NAME	TSSOP	QFN			
ZFLAG	7	24	**Zero Flag Output** 0 = Normal operation 1 = Infinite zero detect is triggered or mute is applied		
DEEMPH	12	5	**De-emphasis Filter Select** 0 = Filter disabled 1 = Filter enabled		
AIFMODE0	13	6	**AIFMODE1**	**AIFMODE0**	**FORMAT**
			0	0	24-bit Left Justified
			0	1	24-bit I^2S
AIFMODE1	14	7	1	0	16-bit Right Justified
			1	1	24-bit Right Justified
$\overline{\text{MUTE}}$	15	8	**Mute Control** 0 = Mute 1 = Normal operation		
CIFMODE	16	9	**Control Interface Mode** 0 = I^2C Mode 1 = SPI Mode Z = Hardware Mode		

Table 22 Hardware Control Pin Configuration

DE-EMPHASIS

A digital de-emphasis filter may be applied to the DAC output when the sampling frequency is 44.1kHz. Operation at 48kHz and 32kHz is also possible, but with an increase in the error from the ideal response. Details of the de-emphasis filter characteristic for 32kHz, 44.1kHz and 48kHz can be seen in Figure 31 to Figure 36.

MUTE

In hardware mode, the $\overline{\text{MUTE}}$ pin controls the DAC mute to both left and right channels. When the mute is asserted a softmute is applied to ramp the signal down, with the ramp rate related to the sample rate as defined in Table 15 on page 28. Once mute is achieved, the ZFLAG is asserted. When the mute is de-asserted the signal returns to full scale in one step and the ZFLAG is de-asserted.

ZERO DETECT

The zero detect function in hardware mode will assert the ZFLAG pin high when 1024 zero count samples are input to the digital audio interface. Additionally, the ZFLAG is asserted when the device is muted using the $\overline{\text{MUTE}}$ pin and also until the device comes out of reset.

POWER UP AND DOWN CONTROL IN HARDWARE MODE

In hardware mode the MCLK, BCLK and $\overline{\text{MUTE}}$ pins are monitored to control how the device powers up or down, and this is summarised in Figure 25 below.

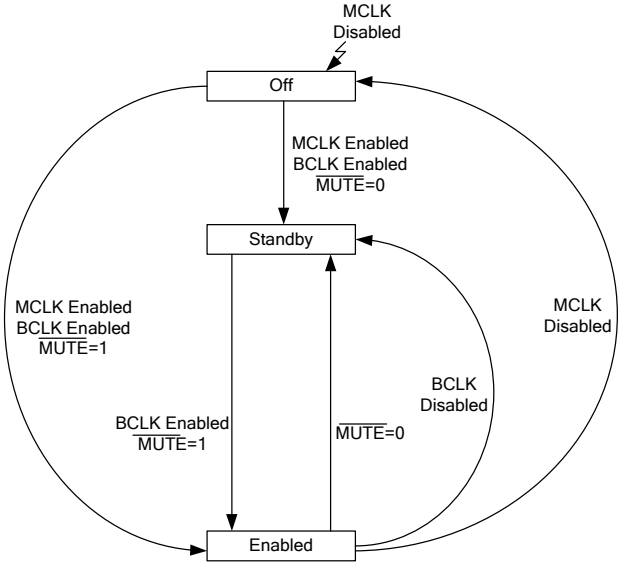


Figure 25 Hardware Power Sequence Diagram

Off to Enable

To power up the device to enabled, start MCLK and BCLK and set $\overline{\text{MUTE}}$ = 1.

Off to Standby

To power up the device to standby, start MCLK and BCLK and set $\overline{\text{MUTE}}$ = 0. Once the device is in standby mode, BCLK can be disabled and the device will remain in standby mode.

Standby to Enable

To transition from the standby state to the enabled state, set the $\overline{\text{MUTE}}$ pin to logic 1 and start BCLK.

Enable to Standby

To power down to a standby state leaving the charge pump running, either set the $\overline{\text{MUTE}}$ pin to logic 0 or stop BCLK. MCLK must continue to run in these situations. The device will automatically mute and power down quietly in either case.

Note: It is recommended that the device is placed in standby mode before sample rate change if the sample rate changes more than once in 1026 LRCLK periods, as detailed in Digital Audio Data Sampling Rates on page 24.

Enable to Off

To power down the device completely, stop MCLK at any time. It is recommended that the device is placed into standby mode as described above before stopping MCLK to allow a quiet shutdown.

For the timing of the off state to enabled state transition (power on to audio out timing), and the enabled state to standby state transition (the shutdown timing), please refer to WTN0302.

POWER DOMAINS

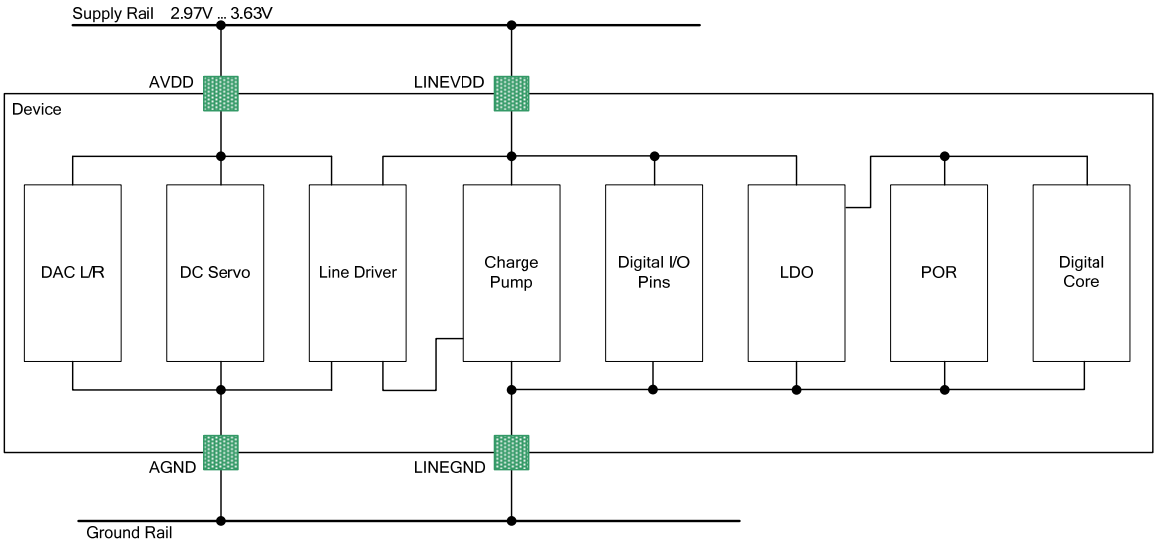


Figure 26 Power Domain Diagram

Power Domain	Name	Blocks Using This Domain	Domain Description
DAC Power Supplies			
3.3V ± 10%	AVDD	Line Driver DAC DC Servo	Analogue Supply
3.3V ± 10%	LINEVDD	Charge Pump Digital LDO Digital Pad buffers	Analogue Supply
Internally Generated Power Supplies and References			
1.65V ± 10%	VMID	DAC, LDO	Ext decoupled resistor string
-3.3V ± 10%	CPVOUTN	Line Driver	Charge pump generated voltage

Table 23 Power Domains

REGISTER MAP

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. The WM8523 can be configured using the Control Interface. All unused bits should be set to '0' and access to unlisted registers should be avoided.

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R0 (0h)	DEVICE_ID / SW RESET	CHIP_ID[15:0]																8523h
R1 (1h)	REVISION	0	0	0	0	0	0	0	0	0	0	0	0	0	CHIP_REV[2:0]			0000h
R2 (2h)	PSCTRL1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SYS_ENA[1:0]		0000h
R3 (3h)	AIF_CTRL1	0	0	0	0	0	0	0	DAC_ DEEMP	AIF_ MSTR	AIF_ LRCLK_ INV	AIF_ BCLK_ INV	AIF_WL[1:0]		0	AIF_FMT[1:0]		1812h
R4 (4h)	AIF_CTRL2	0	0	0	0	0	0	0	0	DAC_OP_MUX[1:0]		AIF_BCLKDIV[2:0]			AIF_SR[2:0]			0000h
R5 (5h)	DAC_CTRL3	0	0	0	0	0	0	0	0	0	0	0	DAC_ZC	DACR_ MUTE	DACL_ MUTE	DAC_ VOL_ UP_ RAMP	DAC_ VOL_ DOWN_ RAMP	0001h
R6 (6h)	DAC_GAINL	0	0	0	0	0	0	DACL_ VU	DACL_VOL[8:0]									0190h
R7 (7h)	DAC_GAINR	0	0	0	0	0	0	DACR_ VU	DACR_VOL[8:0]									0190h
R8 (8h)	ZERO_DETECT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ZD_ COUNT	0000h

Table 24 Register Map

REGISTER BITS BY ADDRESS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R0 (00h) DEVICE_ID/ SW RESET	15:0	CHIP_ID[15:0]	1000_0101_0010_0011	Read this register to obtain Device ID in hex Write any value to this register to reset all register values to default.	Page 18

Register 00h DEVICE_ID / SW RESET

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1 (01h) REVISION	2:0	CHIP_REV[2:0]	000	**Device Revision Number** This number is incrementally updated each time the silicon is revised.	Page 18

Register 01h REVISION

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R2 (02h) PSCTRL1	1:0	SYS_ENA[1:0]	00	**System Power Control** 00 = Off 01 = Power down 10 = Power up to mute 11 = Power up to unmute	Page 25

Register 02h PSCTRL1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R3 (03h) AIF_CTRL1	8	DAC_DEEMP	0	**DAC De-emphasis Control** 0 = No de-emphasis 1 = De-emphasis enabled	Page 29
	7	AIF_MSTR	0	**Master/Slave Select** 0 = Slave mode 1 = Master mode	Page 22
	6	AIF_LRCLK_ INV	0	**LRCLK Inversion Control** 0 = Normal polarity 1 = Inverted polarity When AIF_FMT[2:0]=011 (DSP Mode): 0 = Mode A (2nd clock) 1 = Mode B (1st clock)	Page 22
	5	AIF_BCLK_INV	0	**BCLK Inversion Control** Slave mode: 0 = Use rising edge 1 = Use falling edge Master mode: 0 = BCLK normal 1 = BCLK inverted	Page 22
	4:3	AIF_WL[1:0]	10	**Audio Data Word Length** 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits	Page 22
	2	Reserved	0	Reserved	
	2:0	AIF_FMT[1:0]	10	**Audio Data Interface Format** 00 = Right justified 01 = Left justified 10 = I^2S format 11 = DSP mode	Page 22

Register 03h AIF_CTRL1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R4 (04h) AIF_CTRL2	7:6	DAC_OP_ MUX[1:0]	00	**Digital Monomix Control** 00 = Stereo (normal operation) 01 = Mono (Left data to DACR) 10 = Mono (Right data to DACL) 11 = Digital monomix, (L+R)/2	Page 29
	5:3	AIF_ BCLKDIV[2:0]	000	**BCLK Divider Control (Master Mode)** 000 = MCLK/4 001 = MCLK/8 010 = 32fs 011 = 64fs 100 = 128fs 101 - 111 reserved	Page 22
	2:0	AIF_SR[2:0]	000	**MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs	Page 22

Register 04h AIF_CTRL2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R5 (05h) DAC_CTRL3	4	DAC_ZC	0	**Zero Cross Enable** 0 = Do not use zero cross 1 = Use zero cross	Page 26
	3	DACR_MUTE	0	**Right DAC Mute** 0 = Normal operation 1 = Mute	Page 29
	2	DACL_MUTE	0	**Left DAC Mute** 0 = Normal operation 1 = Mute	Page 29
	1	DAC_VOL_ UP_RAMP	0	**DAC Digital Volume Increase Control** 0 = Apply volume increases instantly (step) 1 = Ramp volume increases	Page 27
	0	DAC_VOL_ DOWN_RAMP	1	**DAC Digital Volume Decrease Control** 0 = Apply volume decreases instantly (step) 1 = Ramp volume decreases	Page 27

Register 05h DAC_CTRL3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R6 (06h) DAC_GAINL	9	DACL_VU	0	**Left DAC Digital Volume Update** 0 = Latch Left DAC volume setting into register map but do not update volume 1 = Latch Left DAC volume setting into register map and update left and right channels simultaneously	Page 26
	8:0	DACL_VOL[8:0]	1_1001_0000	**Left DAC Digital Volume Control** 0 0000 0000 = -100dB 0 0000 0001 = -99.75dB 0 0000 0010 = -99.5dB …0.25dB steps 1 1001 0000 = 0dB …0.25dB steps 1 1011 1110 = +11.75dB 1 11XX XXXX = +12dB	Page 26

Register 06h DAC_GAINL

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R7 (07h) DAC_GAINR	9	DACR_VU	0	**Right DAC Digital Volume Update** 0 = Latch Right DAC volume setting into register map but do not update volume 1 = Latch Right DAC volume setting into register map and update left and right channels simultaneously	Page 26
	8:0	DACR_VOL[8:0]	1_1001_0000	**Right DAC Digital Volume Control** 0 0000 0000 = -100dB 0 0000 0001 = -99.75dB 0 0000 0010 = -99.5dB …0.25dB steps 1 1001 0000 = 0dB …0.25dB steps 1 1011 1110 = +11.75dB 1 11XX XXXX = +12dB	Page 26

Register 07h DAC_GAINR

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R8 (08h) ZERO_ DETECT	0	ZD_COUNT[1:0]	0	**Zero Detect Count Control** 0 = 1024 1 = 2048	Page 29

Register 08h ZERO_DETECT

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Filter – 256fs to 1152fs					
Passband	± 0.1dB			0.454fs	
Passband Ripple				0.1	dB
Stopband		0.546fs			
Stopband attenuation	f > 0.546fs	-50			dB
Group Delay			14.5		Fs
DAC Filter – 128fs and 192fs					
Passband	± 0.1dB			0.247fs	
Passband Ripple				0.1	dB
Stopband		0.753fs			
Stopband attenuation	f > 0.753fs	-50			dB
Group Delay			6.5		Fs

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

DAC FILTER RESPONSES

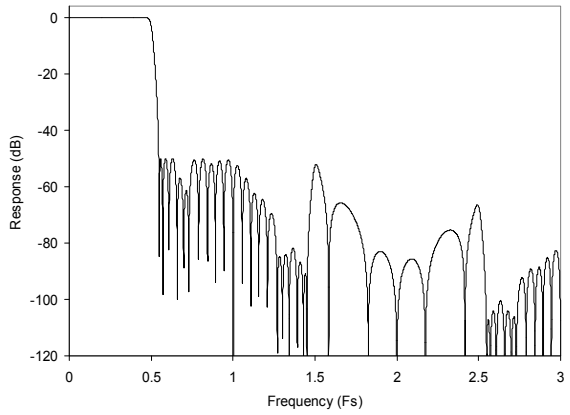


Figure 27 DAC Digital Filter Frequency Response – 256fs to 1152fs Clock Modes

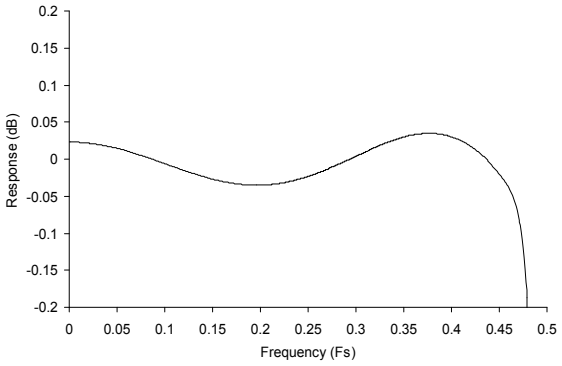


Figure 28 DAC Digital Filter Ripple – 256fs to 1152fs Clock Modes

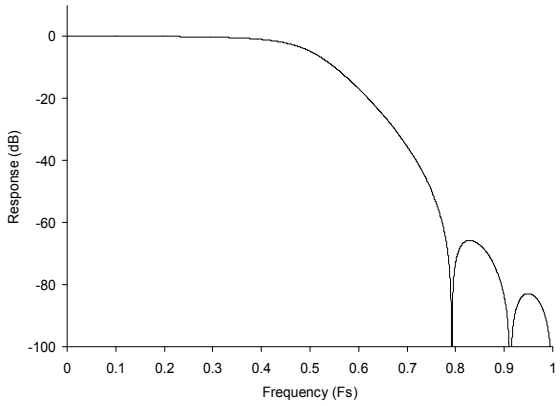


Figure 29 DAC Digital Filter Frequency Response – 128fs and 192fs Clock Modes

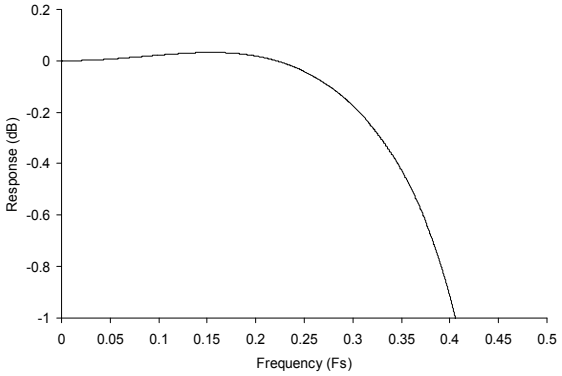


Figure 30 DAC Digital Filter Ripple – 128fs to 192fs Clock Modes

DIGITAL DE-EMPHASIS CHARACTERISTICS

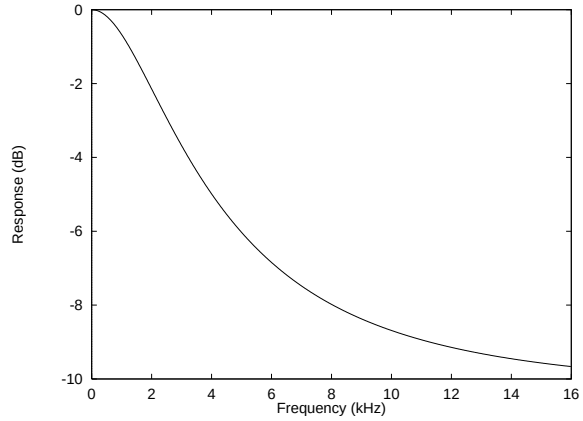


Figure 31 De-Emphasis Frequency Response (32kHz)

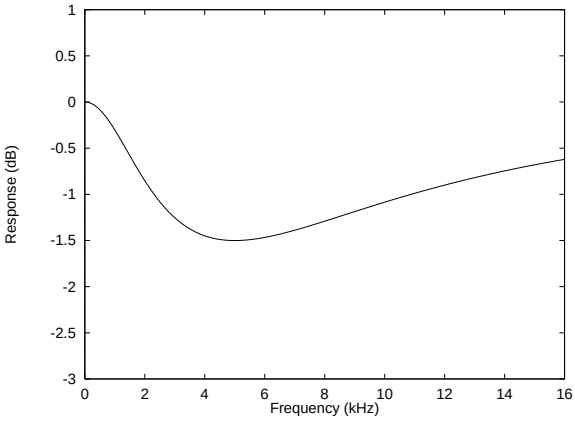


Figure 32 De-Emphasis Error (32kHz)

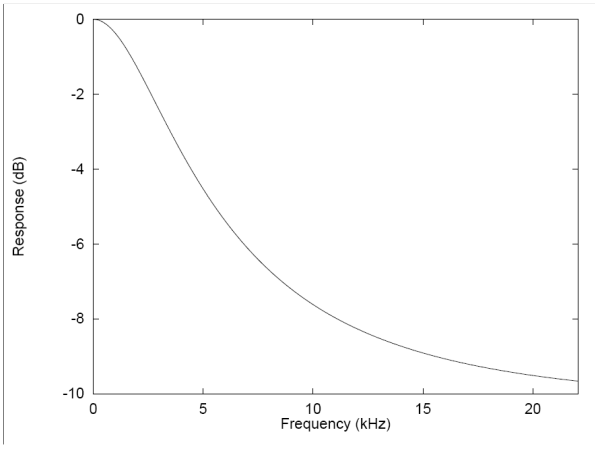


Figure 33 De-Emphasis Frequency Response (44.1kHz)

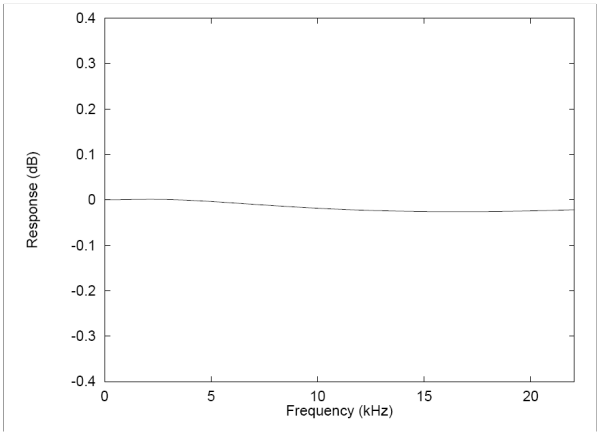


Figure 34 De-Emphasis Error (44.1kHz)

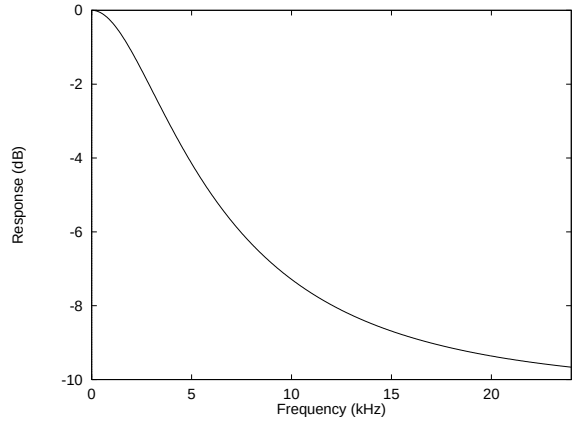


Figure 35 De-Emphasis Frequency Response (48kHz)

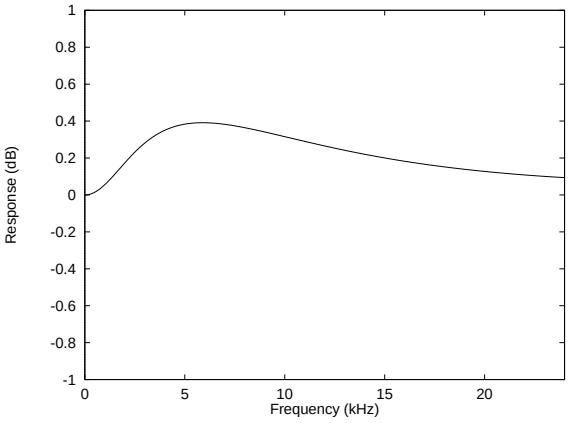


Figure 36 De-Emphasis Error (48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

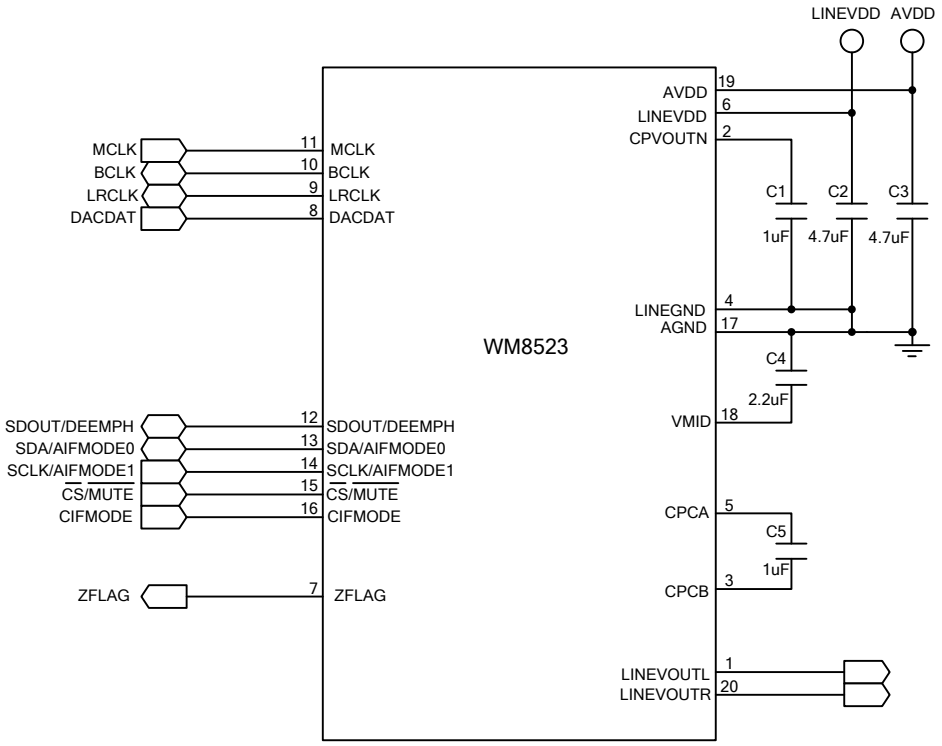


Figure 37 Recommended External Components

Notes:

1. Wolfson recommend using a single, common ground plane. Where this is not possible, care should be taken to optimise split ground configuration for audio performance.
2. Charge Pump fly-back capacitor C5 should be placed as close to WM8523 as possible, followed by Charge Pump decoupling capacitor C1, then LINEVDD and VMID decoupling capacitors. See Recommended PCB Layout on p42.
3. Capacitor types should be chosen carefully. Capacitors with very low ESR are recommended for optimum performance.

RECOMMENDED PCB LAYOUT

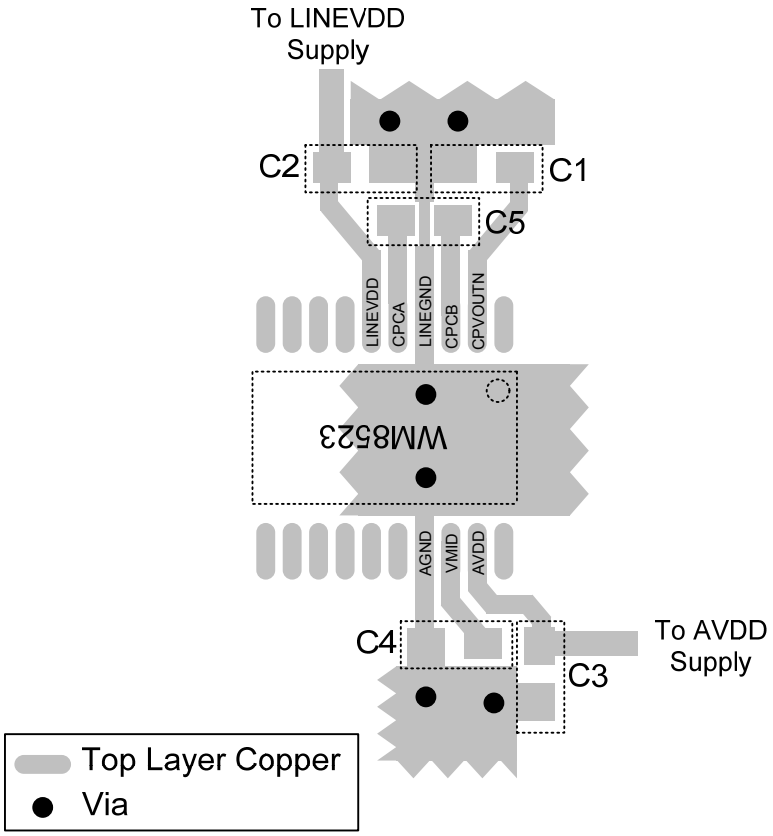


Figure 38 Recommended PCB Layout

Notes:

1. C5 should be placed as close to WM8523 as possible, with minimal track lengths to reduce inductance and maximise performance of the charge pump. Vias should be avoided in the tracking to C5.
2. C1 is then next most important and should also be placed as close as possible to the WM8523. Again, minimise track lengths and avoid vias to reduce parasitic inductance.
3. C2 and C4 are then next most important, and lastly C3.
4. The WM8523 evaluation board, details available at www.wolfsonmicro.com, shows an example of good component placement and layout to maximise performance with a minimal BOM.

RECOMMENDED ANALOGUE LOW PASS FILTER

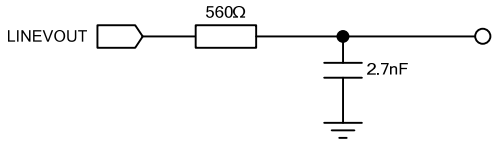


Figure 39 Recommended Analogue Low Pass Filter (one channel shown)

An external single-pole RC filter is recommended if the device is driving a wideband amplifier. Other filter architectures may provide equally good results.

The filter shown in Figure 39 has a -3dB cut-off at 105.26kHz and a droop of 0.15dB at 20kHz. The typical output from the WM8523 is 2.1Vrms – when a 10kΩ load is placed at the output of this recommended filter the amplitude across this load is 1.99Vrms.

RELEVANT APPLICATION NOTES

The following application notes, available from www.wolfsonmicro.com, may provide additional guidance for use of the WM8523.

DEVICE PERFORMANCE:

WAN0129 – Decoupling and Layout Methodology for Wolfson DACs, ADCs and CODECs

WAN0144 – Using Wolfson Audio DACs and CODECs with Noisy Supplies

WTN0302 - WM8524 Recommended Power Sequence and Timing (for hardware mode)

GENERAL:

WAN0108 – Moisture Sensitivity Classification and Plastic IC Packaging

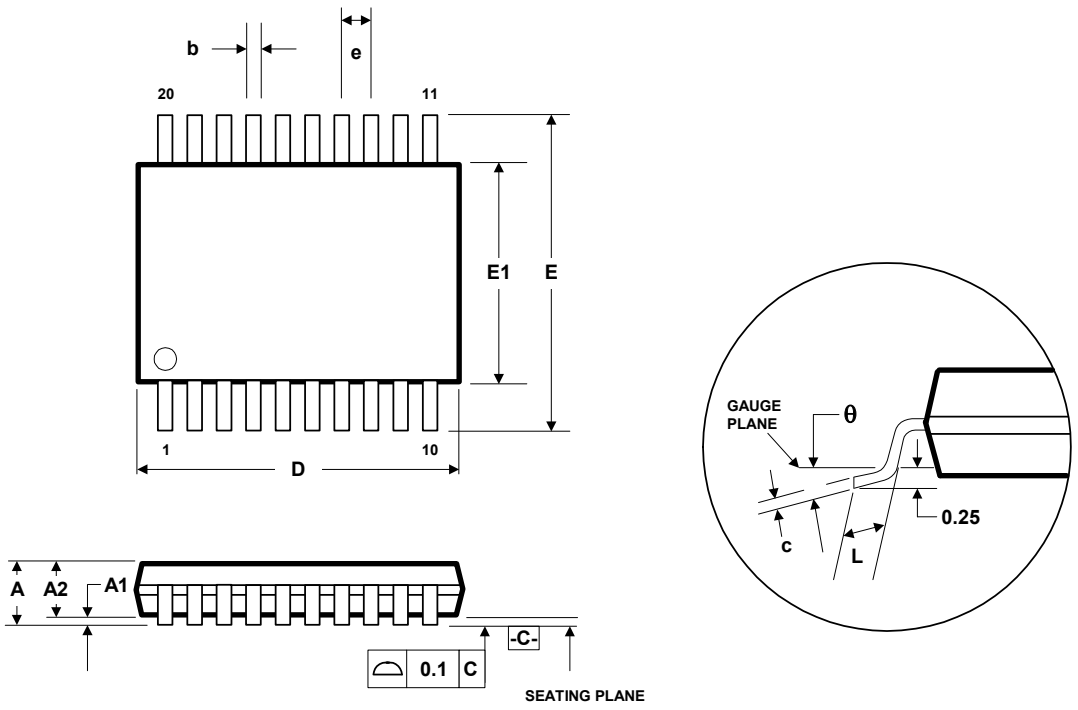
WAN0109 – ESD Damage in Integrated Circuits: Causes and Prevention

WAN0158 – Lead-Free Solder Profiles for Lead-Free Components

WAN0161 – Electronic End-Product Design for ESD

PACKAGE DIMENSIONS

DT: 20 PIN TSSOP (6.5 x 4.4 x 1.0 mm) **DM008.D**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.80	1.00	1.05
b	0.19	-----	0.30
c	0.09	-----	0.20
D	6.40	6.50	6.60
e	0.65 BSC		
E	6.4 BSC		
E_1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ	0^o	-----	8^o
REF:	JEDEC.95, MO-153		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MO-153, VARIATION = AC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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ADDRESS

Wolfson Microelectronics plc

Westfield House

26 Westfield Road

Edinburgh

EH11 2QB

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: apps@wolfsonmicro.com

REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES	PAGE
23/08/10	4.1	BT	Added minimum A-weighted SNR limit of 100dB	9
		BT	Changed Group delay of 256/128fs filters from 10fs to 14.5fs and 6.5fs	40
05/07/13	4.2	JMacD	QFN part removed from datasheet.	various